Theory of Semiconductor Devices (반도체 소자 이론)

Chapter 12. Fundamentals of the MOSFET (1)

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Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

The single-junction semiconductor devices, including the pn homojunction diode, can be used to produce rectifying current-voltage characteristics and to form electronic switching circuits.

The transistor is a multijunction semiconductor device that, in conjunction with other circuit elements, is capable of current gain, voltage gain, and signal power gain. The basic transistor action is the control of current at one terminal by the voltage applied across the other two terminals of the device.

The MOSFET is one of two major types of transistors. The MOSFET is used extensively in digital circuit applications where, because of its small size, millions of device can be fabricated in a single integrated circuit.

The metal-insulator-semiconductor (MIS) capacitor is the most useful device in the study of semiconductor surfaces. Since most practical problems in the reliability and stability of all semiconductor devices are intimately related to their surface conditions, an understanding of the surface physics with the help of MIS capacitors is of great importance to device operations.

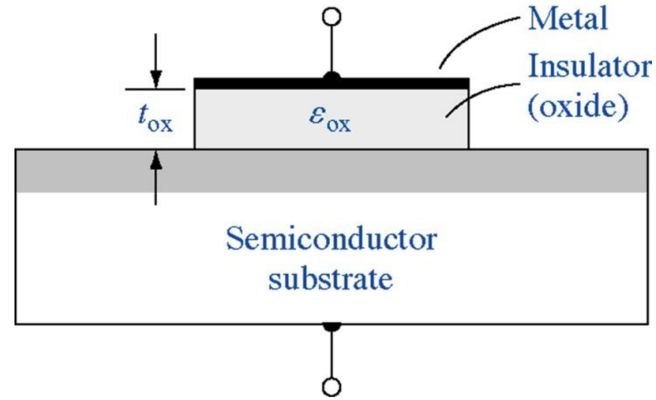
The MOS system has been extensively studied because it is directly related to most silicon planar devices and integrated circuits.

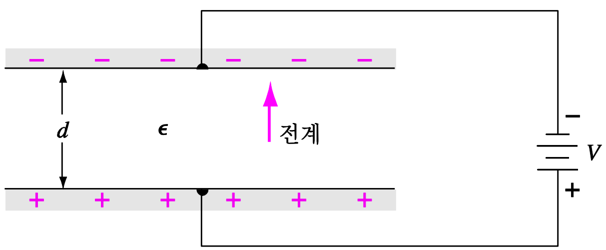
Energy Band Diagram of MOS Capacitor

M : Metal or heavy-doped Poly-(Crystalline) Silicon

O : Oxide (SiO_2) or high-*k* dielectric material

S : Semiconductor (Silicon)





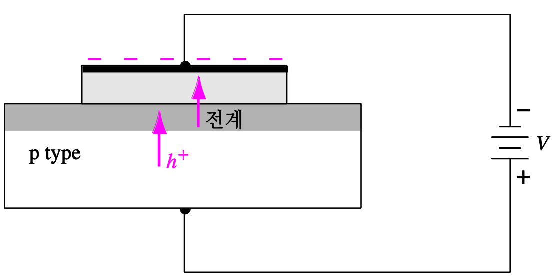
Parallel plate capacitor

$$C' = \frac{\epsilon}{d}$$

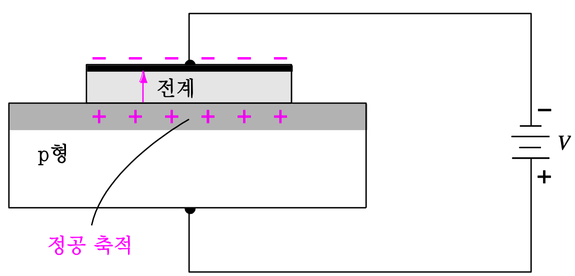
C' : capacitance per unit area

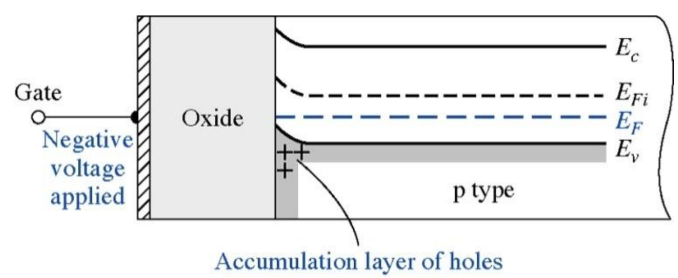
$$Q' = C'V \qquad \mathrm{E} = \frac{V}{d}$$

Negatively biased MOS Capacitor



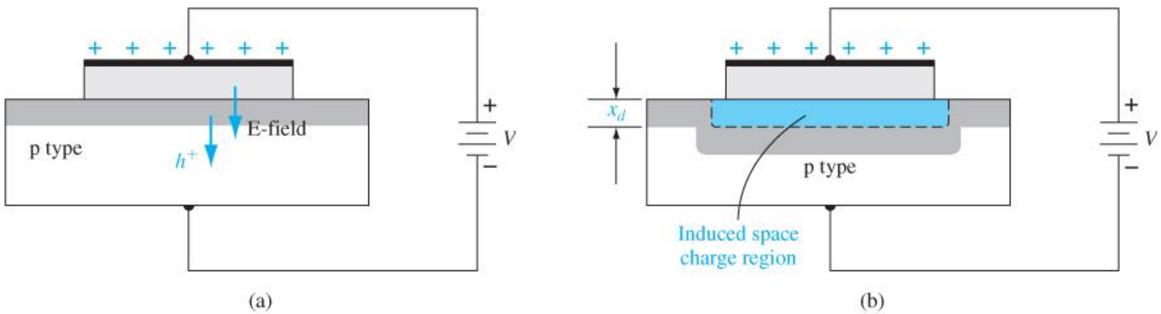
MOS capacitor with Negative Gate bias





Accumulated Hole layer at oxide-semiconductor interface.

Moderately Positive-biased MOS Capacitor



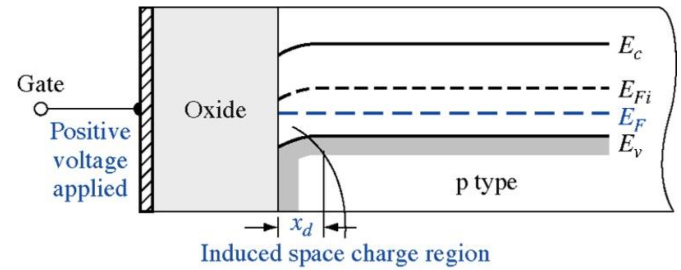
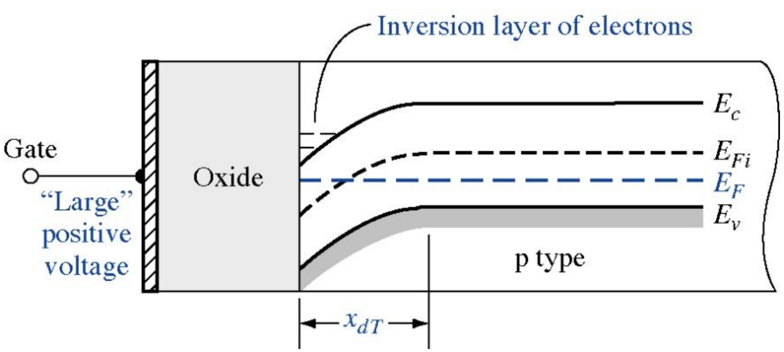


Figure 10.3 | The MOS capacitor with a moderate positive gate bias, showing (a) the electric field and charge flow and (b) the induced space charge region.

Large Positive-biased MOS Capacitor



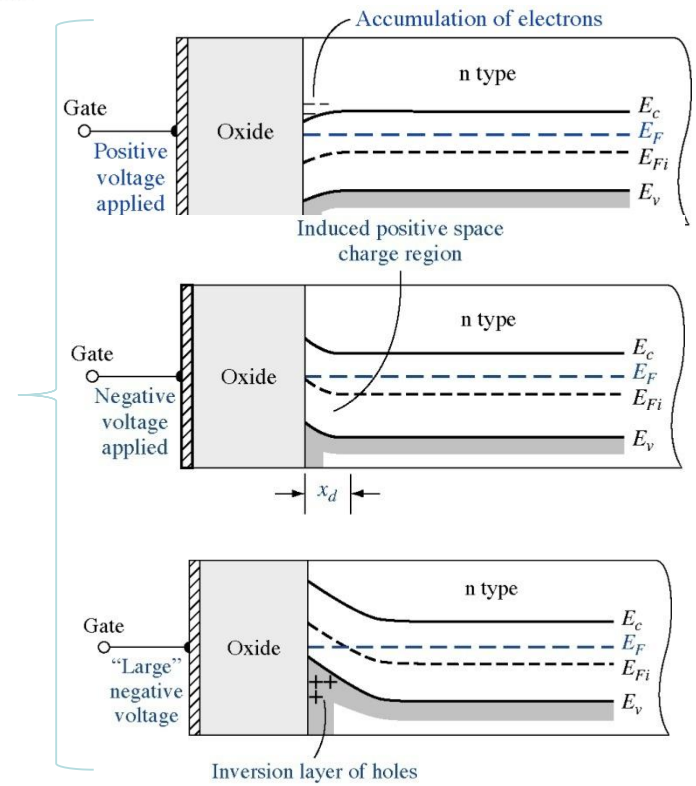
Induced Inversion layer at the interface

MOS Capacitor with n-type substrate for

a positive,

moderate-negative, and

strong negative gate bias.



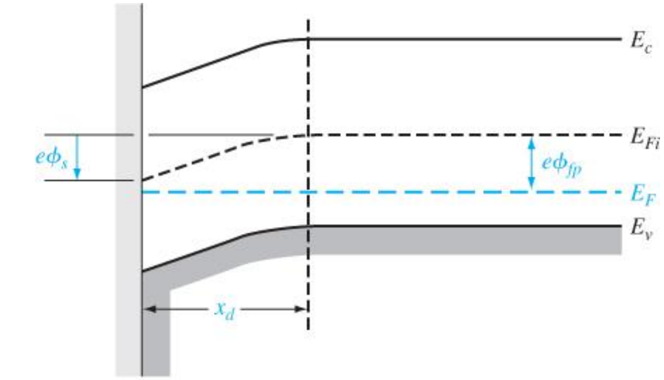
Depletion Layer Thickness

$$N_a = n_i \exp\left[\frac{E_{Fi} - E_F}{kT}\right] \Rightarrow \phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right)$$

$$W \approx \left\{\frac{2\epsilon_s(V_{bi} + V_R)}{eN_d}\right\}^{1/2} \Rightarrow x_d = \left(\frac{2\epsilon_s \phi_s}{eN_a}\right)^{1/2}$$

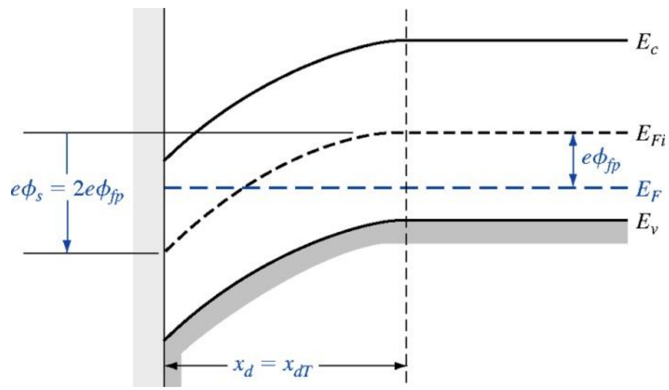
ϕ_s : Surface Potential

One-sided step junction



Threshold inversion point : $\phi_s = 2\phi_{fp} \Rightarrow x_{dT} = \left(\frac{4\epsilon_s \phi_{fp}}{eN_a}\right)^{1/2}$

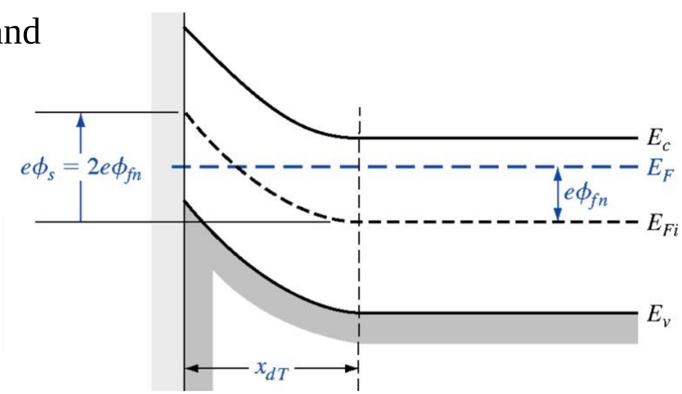
: maximum space charge width



Threshold Voltage : the applied gate bias voltage for $\phi_s = 2\phi_{fp}$

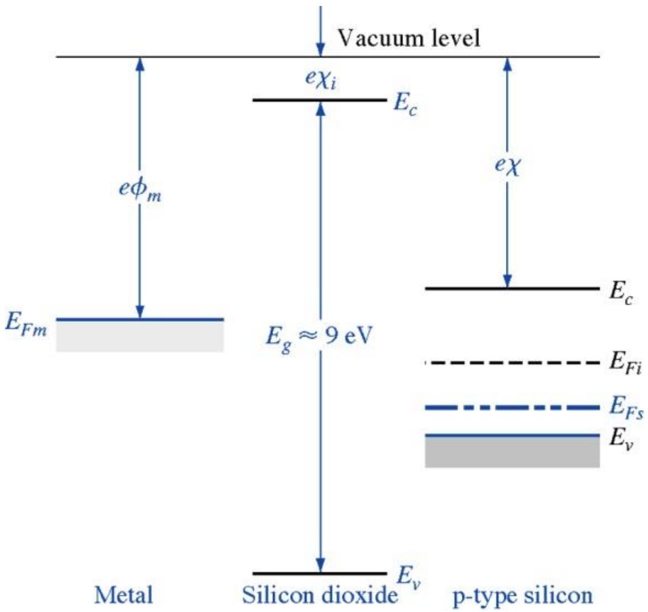
: inversion carrier density = bulk majority carrier density

Change of applied gate bias voltage. → slight change of surface potential and space charge width, but exponential change of inversion charge density !!

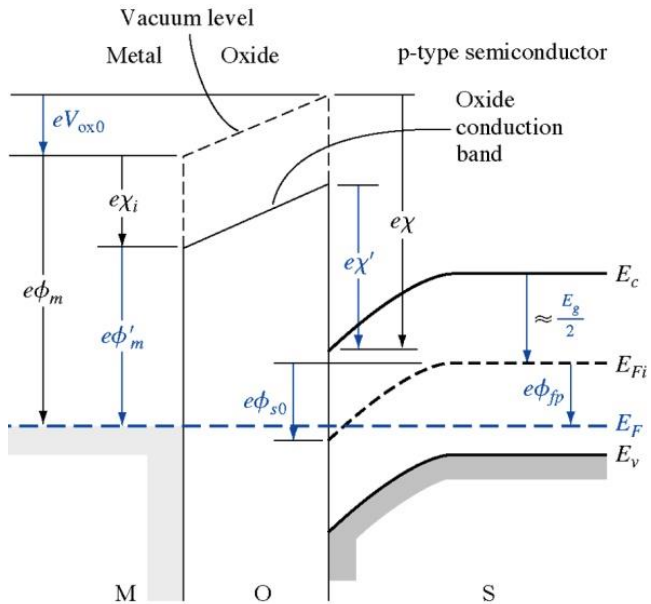


For n-type substrate : $\phi_{fn} = V_t \ln\left(\frac{N_d}{n_i}\right) \quad x_{dT} = \left(\frac{4\epsilon_s \phi_{fn}}{eN_d}\right)^{1/2}$

Work Function Differences



Before contact



Thermal equilibrium after contact

$\phi'_m = \phi_m - \chi_i$

$\chi' = \chi - \chi_i$

χ_i : electron affinity of oxide

V_{ox0} : potential drop across oxide at equilibrium

$$e\phi'_m + eV_{ox0} = e\chi' + \frac{E_g}{2} - e\phi_{s0} + e\phi_{fp} \Longrightarrow V_{ox0} + \phi_{s0} = -\left[\phi'_m - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right)\right] = -\phi_{ms}$$

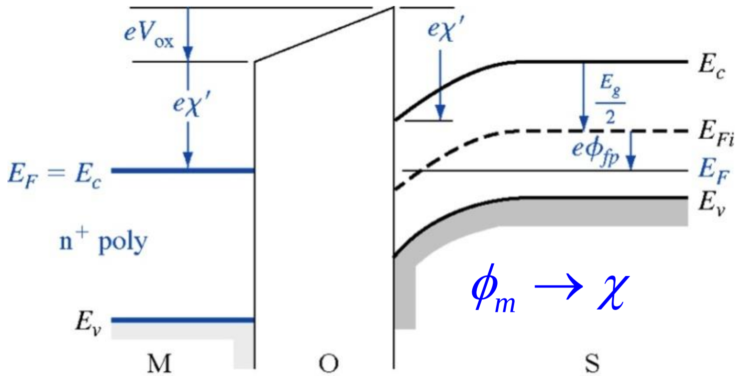
$$\phi_{ms} \equiv \phi_m - \phi_s = \left(\phi'_m + \chi_i\right) - \left(\chi + \frac{E_g}{2e} + \phi_{fp}\right) = \phi'_m - \left(\chi - \chi_i + \frac{E_g}{2e} + \phi_{fp}\right) = \left[\phi'_m - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right)\right]$$

: Metal-semiconductor work function difference

Work Function Differences : Poly-silicon gate

$$\phi'_m = \phi_m - \chi_i$$
$$\chi' = \chi - \chi_i$$

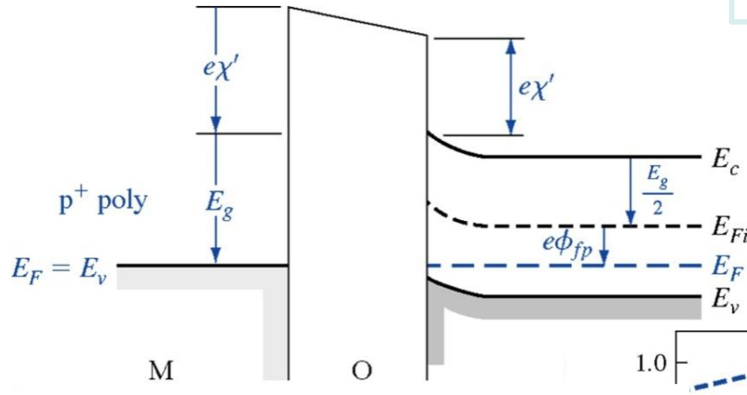
n^+ poly-Si Gate



$$\phi_m \rightarrow \chi$$

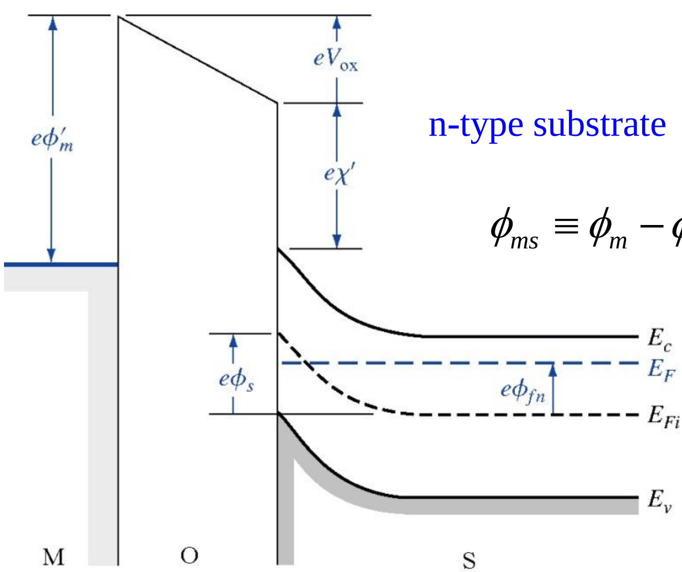
$$\phi_{ms} = \left[\chi' - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right)\right] = -\left(\frac{E_g}{2e} + \phi_{fp}\right)$$

p^+ poly-Si Gate



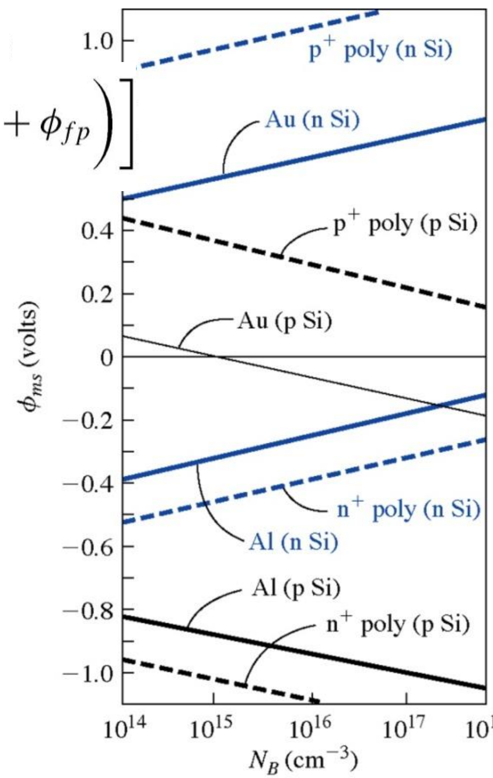
$$\phi_m \rightarrow \chi + \frac{E_g}{e}$$

$$\phi_{ms} = \left[\left(\chi' + \frac{E_g}{e}\right) - \left(\chi' + \frac{E_g}{2e} + \phi_{fp}\right)\right]$$
$$= \left(\frac{E_g}{2e} - \phi_{fp}\right)$$



n-type substrate

$$\phi_{ms} \equiv \phi_m - \phi_s = \left(\phi'_m + \chi_i\right) - \left(\chi + \frac{E_g}{2e} - \phi_{fn}\right)$$
$$= \phi'_m - \left(\chi' + \frac{E_g}{2e} - \phi_{fn}\right)$$



Flat-Band Voltage

: the applied gate voltage such that there is no band bending in the semiconductor region (zero net space charge)

- Band bending in equilibrium : work function difference and the oxide charge → Need a voltage for the band to be Flat..

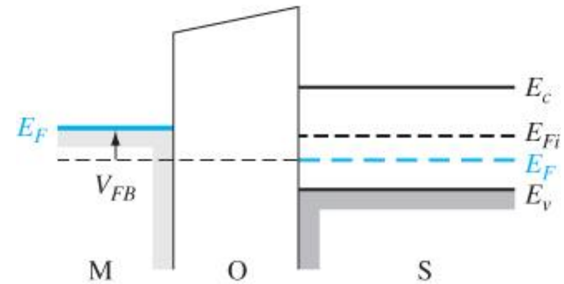
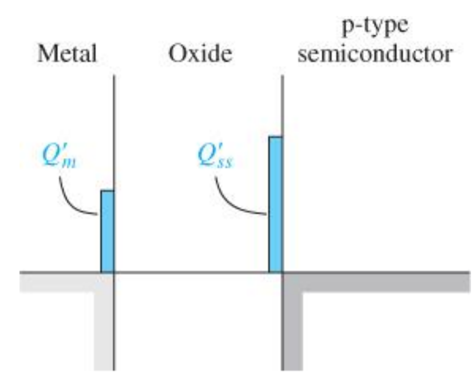


Figure 10.17 | Energy-band diagram of a MOS capacitor at flat band.

For zero applied gate voltage : $$V_{ox0} + \phi_{s0} = -\phi_{ms}$$

When V_G is applied to the gate : $$V_G = \Delta V_{ox} + \Delta\phi_s = (V_{ox} - V_{ox0}) + (\phi_s - \phi_{s0})$$
$$= V_{ox} + \phi_s + \phi_{ms}$$

Charge distribution at flat band



When the flat-band voltage is applied to the gate :

$$Q'_m + Q'_{ss} = 0 \qquad V_{ox} = \frac{Q'_m}{C_{ox}} \qquad V_{ox} = \frac{-Q'_{ss}}{C_{ox}}$$

Q'_{ss} : the equivalent oxide charge at the interface

$$V_G = V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}}$$

Example 11.3 : MOS capacitor with $N_a = 10^{16}$ cm^{-3}, $t_{ox} = 500$ Å and n^+ poly-Si gate. $Q'_{ss} = 10^{11}$ cm^{-2}.

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.85 \times 10^{-14})}{500 \times 10^{-8}} = 6.9 \times 10^{-8} \text{ F/cm}^2$$

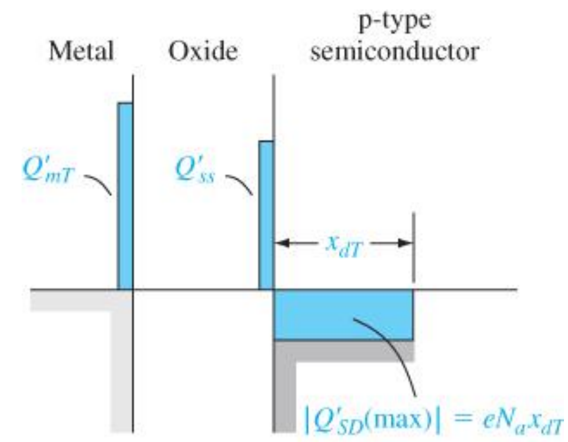
$$Q'_{ss} = (10^{11})(1.6 \times 10^{-19}) = 1.6 \times 10^{-8} \text{ C/cm}^2$$

$$V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}} = -1.1 - \left(\frac{1.6 \times 10^{-8}}{6.9 \times 10^{-8}}\right) = -1.33 \text{ V}$$

Threshold Voltage

: the applied gate voltage required to achieve the threshold inversion point. $\phi_s = 2\phi_{fp}$ or $\phi_s = 2\phi_{fn}$.

Assume $Q'_{inv} << Q'_{SD}(\max)$



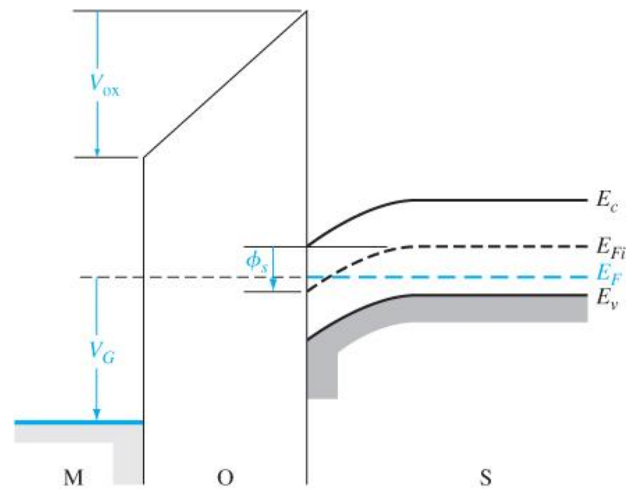
$$|Q'_{SD}(\max)| = eN_a x_{dT} \qquad Q'_{mT} + Q'_{ss} = |Q'_{SD}(\max)|$$

Q'_{mT} : the positive charge at the metal side at threshold

$$V_G = \Delta V_{\text{ox}} + \Delta\phi_s = V_{\text{ox}} + \phi_s + \phi_{ms}$$

At threshold, $V_G = V_{TN}$: $\quad V_{TN} = V_{\text{ox}T} + 2\phi_{fp} + \phi_{ms}$

V_{oxT} : the voltage across the oxide at threshold inversion point



$$V_{\text{ox}T} = \frac{Q'_{mT}}{C_{\text{ox}}} = \frac{Q'_{mT}}{C_{\text{ox}}} = \frac{1}{C_{\text{ox}}}(|Q'_{SD}(\max)| - Q'_{ss})$$

$$V_{TN} = \frac{|Q'_{SD}(\max)|}{C_{\text{ox}}} - \frac{Q'_{ss}}{C_{\text{ox}}} + \phi_{ms} + 2\phi_{fp}$$

$$= (|Q'_{SD}(\max)| - Q'_{ss})\left(\frac{t_{\text{ox}}}{\epsilon_{\text{ox}}}\right) + \phi_{ms} + 2\phi_{fp}$$

$$= \frac{|Q'_{SD}(\max)|}{C_{\text{ox}}} + V_{FB} + 2\phi_{fp}$$

For a given semiconductor material, oxide material, and gate metal, the threshold voltage is a function of semiconductor doping, oxide charge density and oxide thickness.

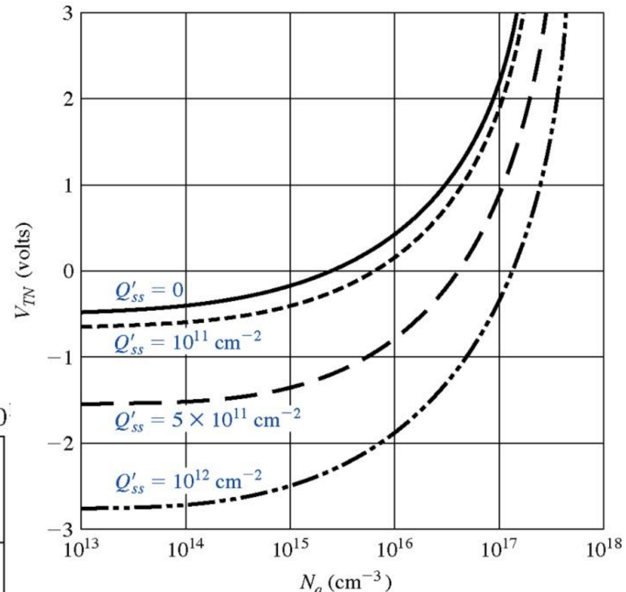
Example 11.3 : MOS capacitor with Al gate, $N_a = 10^{14}$ cm^{-3}, $t_{ox} = 500$ Å. $Q'_{ss} = 10^{10}$ cm^{-2}. $\phi_{ms} = -0.83$V

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = (0.0259)\ln\left(\frac{10^{14}}{1.5\times10^{10}}\right) = 0.228 \text{ V}$$

$$x_{dT} = \left\{\frac{4\epsilon_s\phi_{fp}}{eN_a}\right\}^{1/2} = \left\{\frac{4(11.7)(8.85\times10^{-14})(0.228)}{(1.6\times10^{-19})(10^{14})}\right\}^{1/2} = 2.43\ \mu\text{m}$$

$$|Q'_{SD}(\text{max})| = eN_a x_{dT} = (1.6\times10^{-19})(10^{14})(2.43\times10^{-4})$$
$$= 3.89\times10^{-9} \text{ C/cm}^2$$

$$V_{TN} = (|Q'_{SD}(\text{max})| - Q'_{ss})\left(\frac{t_{ox}}{\epsilon_{ox}}\right) + \phi_{ms} + 2\phi_{fp}$$
$$= [(3.89\times10^{-9}) - (10^{10})(1.6\times10^{-19})]\left[\frac{500\times10^{-8}}{(3.9)(8.85\times10^{-14})}\right]$$
$$-0.83 + 2(0.228)$$
$$= -0.341 \text{ V}$$



For a MOS capacitor with n-type semiconductor substrate :

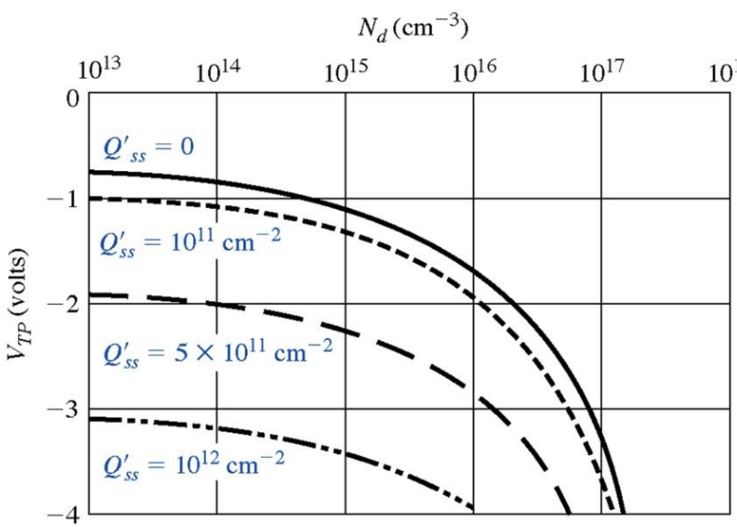
$$V_{TP} = (-|Q'_{SD}(\text{max})| - Q'_{ss})\left(\frac{t_{ox}}{\epsilon_{ox}}\right) + \phi_{ms} - 2\phi_{fn}$$

$$\phi_{ms} = \phi'_m - \left(\chi' + \frac{E_g}{2e} - \phi_{fn}\right)$$

$$|Q'_{SD}(\text{max})| = eN_d x_{dT}$$

$$x_{dT} = \left\{\frac{4\epsilon_s\phi_{fn}}{eN_d}\right\}^{1/2}$$

$$\phi_{fn} = V_t \ln\left(\frac{N_d}{n_i}\right)$$



Threshold voltage vs. Substrate doping concentration (depending on Q'_{ss})

Charge Distribution

$$n_s = n_0 \exp\left(\frac{\phi_s}{V_t}\right) = \frac{n_i^2}{N_a} \exp\left(\frac{\phi_s}{V_t}\right)$$

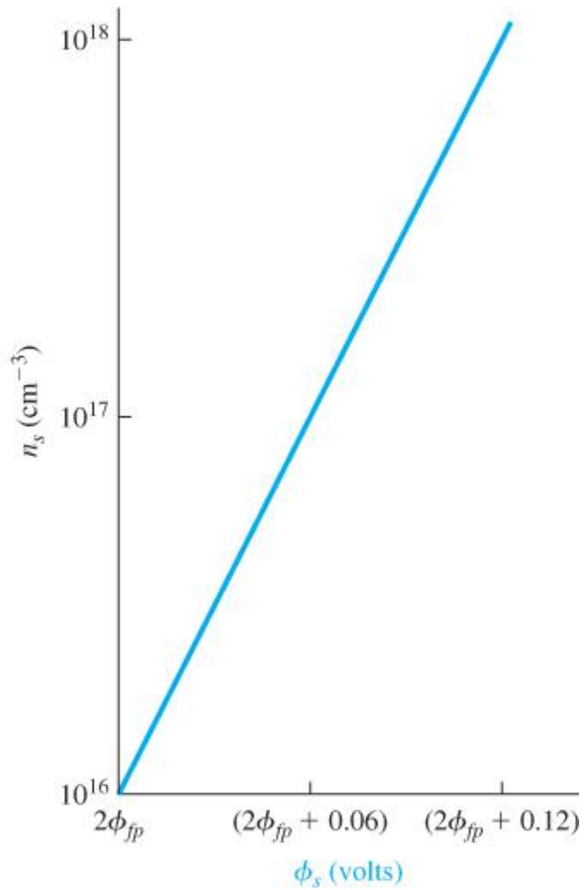
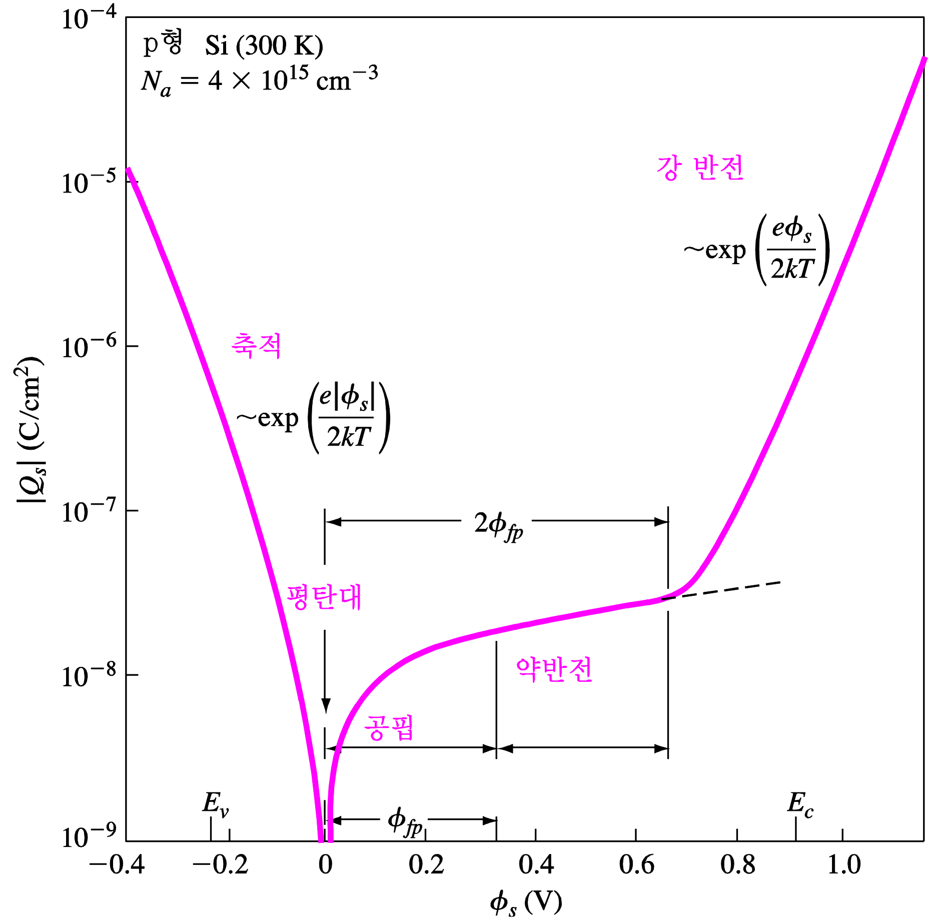


Figure 10.12 | Electron inversion charge density as a function of surface potential.

Surface charge density in the silicon region as a function of ϕ_s



Capacitance

$$C = \frac{dQ}{dV}$$

dQ : magnitude of the differential change in charge on one plate

dV : differential voltage change across the capacitor

$$C'(\mathrm{acc}) = C_{\mathrm{ox}} = \frac{\epsilon_{\mathrm{ox}}}{t_{\mathrm{ox}}}$$

Accumulation mode

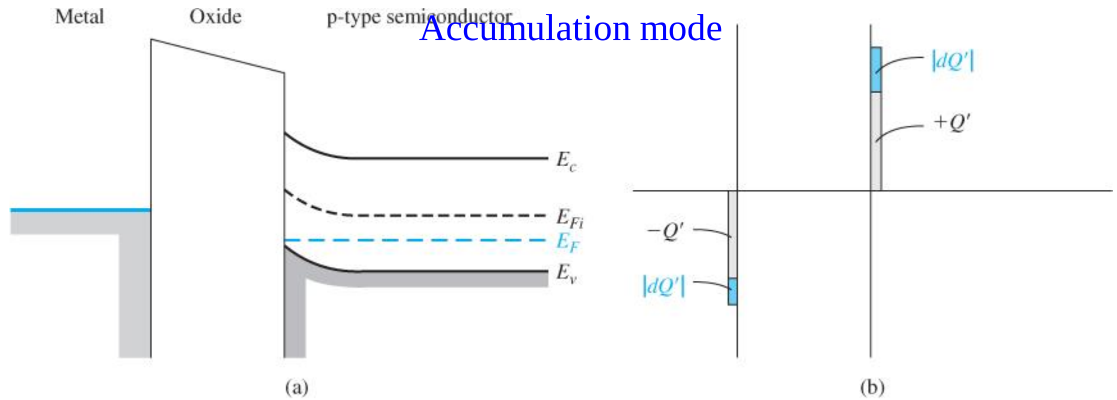


Figure 10.23 | (a) Energy-band diagram through a MOS capacitor for the accumulation mode. (b) Differential charge distribution at accumulation for a differential change in gate voltage.

$$\frac{1}{C'(\mathrm{depl})} = \frac{1}{C_{\mathrm{ox}}} + \frac{1}{C'_{SD}}$$

$$C'(\mathrm{depl}) = \frac{C_{\mathrm{ox}} C'_{SD}}{C_{\mathrm{ox}} + C'_{SD}} \qquad C'_{SD} = \frac{\varepsilon_s}{x_d}$$

$$C'(\mathrm{depl}) = \frac{C_{\mathrm{ox}}}{1 + \dfrac{C_{\mathrm{ox}}}{C'_{SD}}} = \frac{\epsilon_{\mathrm{ox}}}{t_{\mathrm{ox}} + \left(\dfrac{\epsilon_{\mathrm{ox}}}{\epsilon_s}\right) x_d}$$

Depletion mode

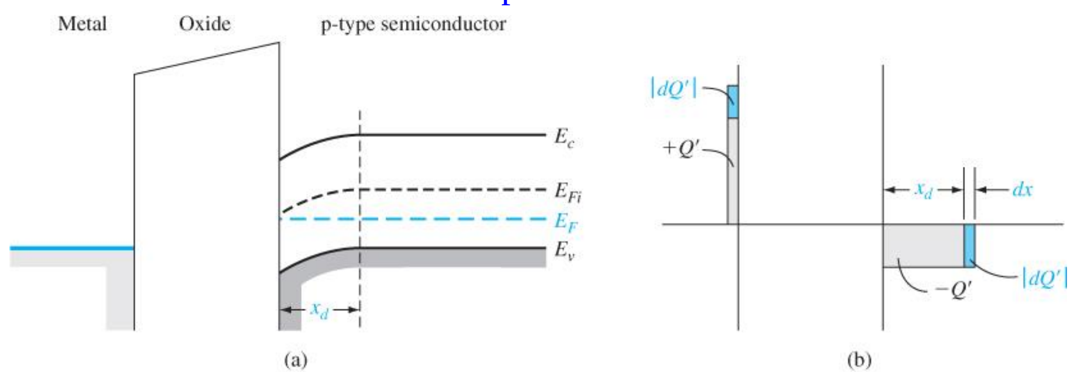


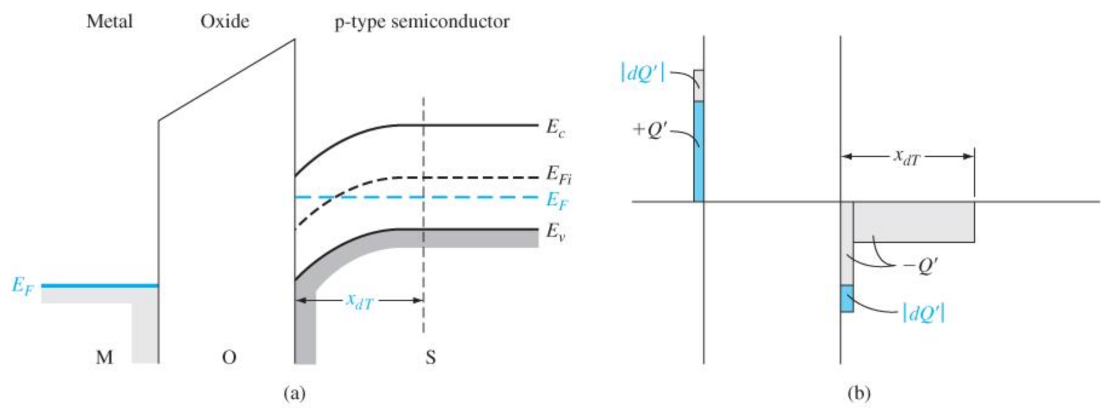
Figure 10.24 | (a) Energy-band diagram through a MOS capacitor for the depletion mode. (b) Differential charge distribution at depletion for a differential change in gate voltage.

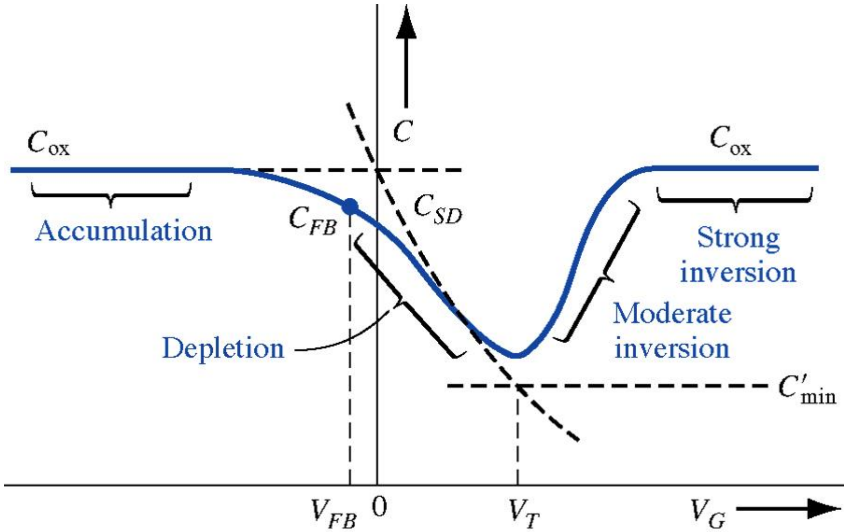
$$C'_{min} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right) x_{dT}}$$

: Maximum depletion width and essentially zero (assumed) inversion charge

$$C'(\text{inv}) = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

Inversion mode





Example 11.3 : MOS capacitor with $N_a = 10^{16}$ cm^{-3}, $t_{ox} = 550$ Å and Aluminum gate.

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{(3.9)(8.85 \times 10^{-14})}{550 \times 10^{-8}} = 6.28 \times 10^{-8} \text{ F/cm}^2$$

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right) = (0.0259) \ln\left(\frac{10^{16}}{1.5 \times 10^{10}}\right) = 0.347 \text{ V}$$

$$x_{dT} = \left\{\frac{4\epsilon_s \phi_{fp}}{eN_a}\right\}^{1/2} = \left\{\frac{4(11.7)(8.85 \times 10^{-14})(0.347)}{(1.6 \times 10^{-19})(10^{16})}\right\}^{1/2} = 0.30 \times 10^{-4} \text{ cm}$$

$$C'_{min} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right) x_{dT}} = \frac{(3.9)(8.85 \times 10^{-14})}{(550 \times 10^{-8}) + \left(\frac{3.9}{11.7}\right)(0.3 \times 10^{-4})} = 2.23 \times 10^{-8} \text{ F/cm}^2$$

$$\frac{C'_{min}}{C_{ox}} = \frac{2.23 \times 10^{-8}}{6.28 \times 10^{-8}} = 0.355$$

Frequency Effects

Two sources of inversion charge (electron)

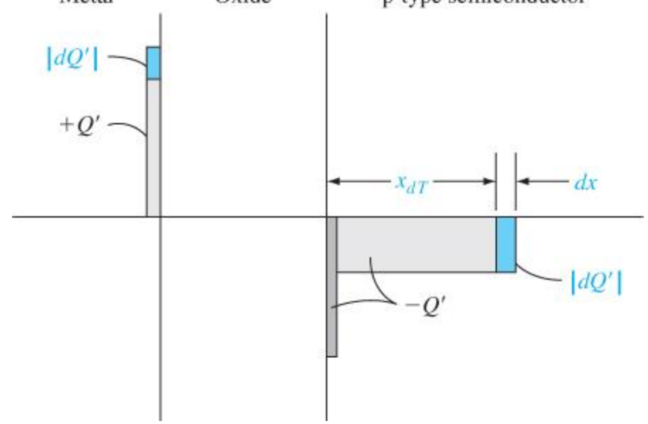
1. Diffused minority carrier electrons from the p-type substrate across the space charge region.
2. Thermally generated electron-hole pair within the space charge region.

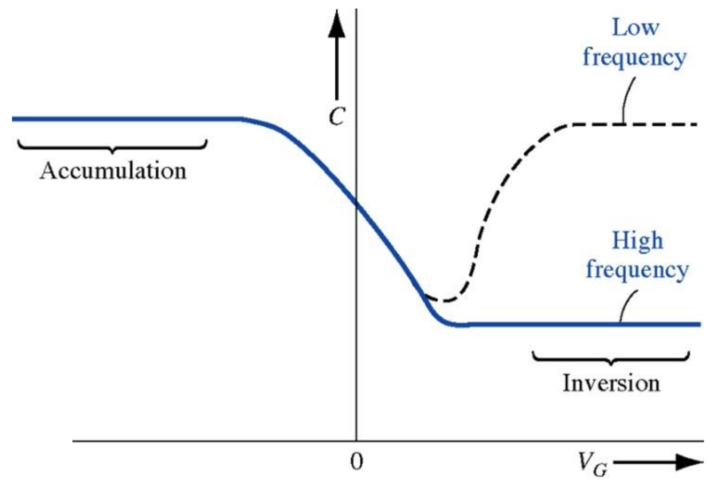
→ Both of these processes generates electrons at a particular rate.

→ The electron concentration in inversion layer cannot change instantaneously.

→ At a high frequency, the differential change in charge occurs at the metal and in the space charge width in the semiconductor

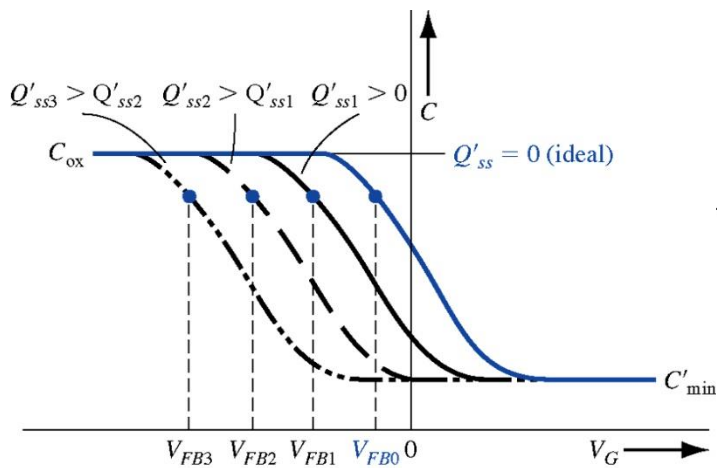
Inversion mode at high-frequency





Fixed Oxide Effects

$$V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}}$$



Carrier transport

In an ideal MIS capacitor the conductance of the insulating film is assumed to be zero.

Real insulators, however, show some degree of carrier conduction when the electric field or temperature is sufficiently high.

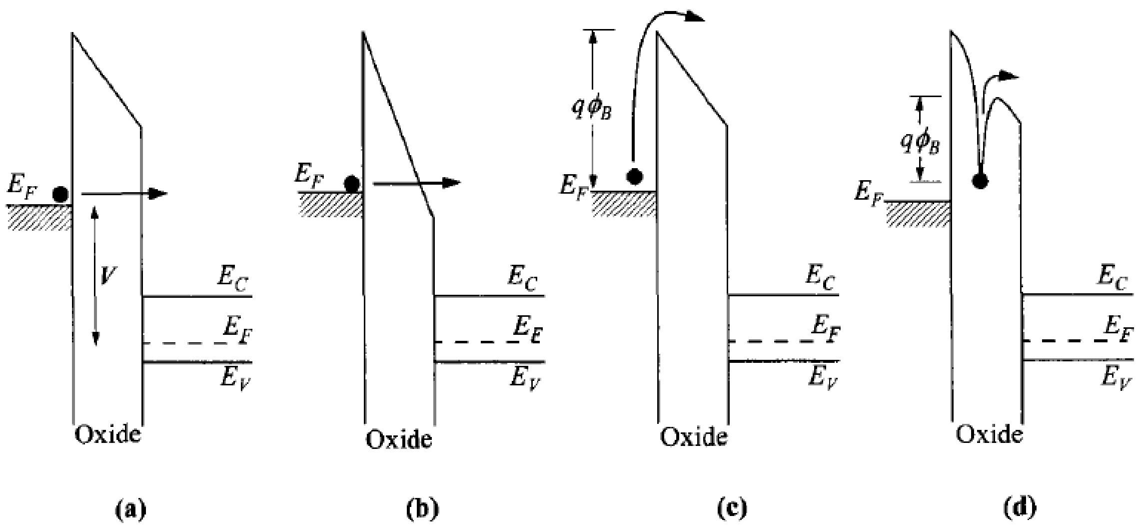


Fig. 23 Energy-band diagrams showing conduction mechanisms of (a) direct tunneling, (b) Fowler-Nordheim tunneling, (c) thermionic emission, and (d) Frenkel-Poole emission.

Tunneling can be divided into direct tunneling and Fowler-Nordheim tunneling where carriers tunnel through only a partial width of the barrier.

The Frenkel-Poole emission is due to emission of trapped electrons into the conduction band. The supply of electrons from the traps is through thermal excitation.

Carrier transport

Table 2 Basic Conduction Processes in Insulators

Process	Expression	Voltage & temperature dependence
Tunneling	$J \propto \mathscr{E}_i^2 \exp\left[-\frac{4\sqrt{2m^*}(q\phi_B)^{3/2}}{3q\hbar\mathscr{E}_i}\right]$	$\propto V^2 \exp\left(\frac{-b}{V}\right)$
Thermionic emission	$J = A^{**}T^2 \exp\left[\frac{-q(\phi_B - \sqrt{q\mathscr{E}_i/4\pi\varepsilon_i})}{kT}\right]$	$\propto T^2 \exp\left[\frac{q}{kT}(a\sqrt{V} - \phi_B)\right]$
Frenkel-Poole emission	$J \propto \mathscr{E}_i \exp\left[\frac{-q(\phi_B - \sqrt{q\mathscr{E}_i/\pi\varepsilon_i})}{kT}\right]$	$\propto V \exp\left[\frac{q}{kT}(2a\sqrt{V} - \phi_B)\right]$
Ohmic	$J \propto \mathscr{E}_i \exp\left(\frac{-\Delta E_{ac}}{kT}\right)$	$\propto V \exp\left(\frac{-c}{T}\right)$
Ionic conduction	$J \propto \frac{\mathscr{E}_i}{T} \exp\left(\frac{-\Delta E_{ai}}{kT}\right)$	$\propto \frac{V}{T} \exp\left(\frac{-d'}{T}\right)$
Space-charge-limited	$J = \frac{9\varepsilon_i \mu V^2}{8d^3}$	$\propto V^2$

A^{**} = effective Richardson constant. ϕ_B = barrier height. $\mathscr{E}_i$ = electric field in insulator. ε_i = insulator permittivity. $m*$ = effective mass. d = insulator thickens. ΔE_{ac} = activation energy of electrons. ΔE_{ai} = activation energy of ions. $V \approx \mathscr{E}_i d$. $a \equiv \sqrt{q/4\pi\varepsilon_i d}$. b, c, and d' are constants.

For a given insulator, each conduction process may dominate in certain temperature and voltage range. The processes are also not exactly independent of one another and should be carefully examined.

Carrier transport

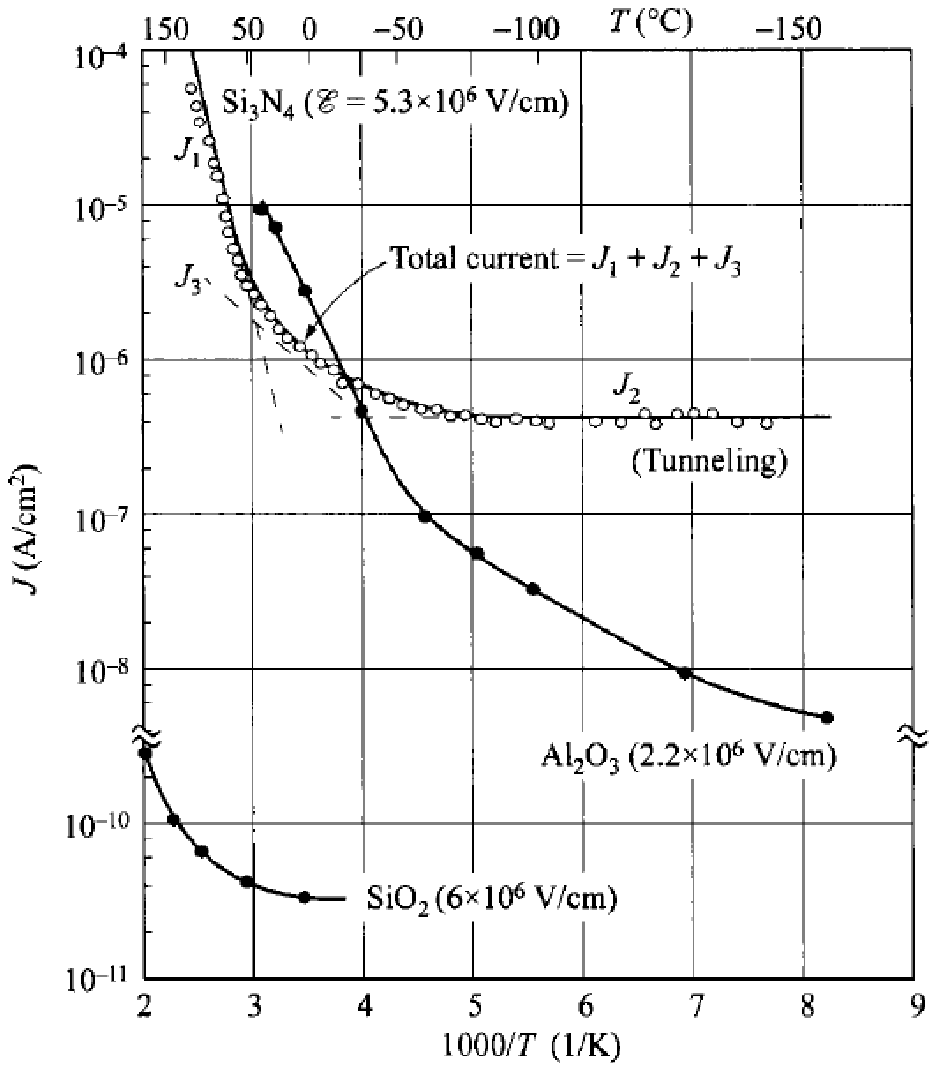


Fig. 24 Current density vs. $1/T$ for Si_3N_4, Al_2O_3, and SiO_2 films. (After Refs. 35–37.)