

## Improved light extraction efficiency of GaN-based vertical LEDs using hierarchical micro/subwavelength structures

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We demonstrate the hierarchical micro- and subwavelength-structures on the surface of GaN based green vertical light-emitting diodes (VLEDs) to enhance the light extraction efficiency. Hierarchical structures (HSs), which were fabricated by simple two-step process consisting of pattern transfer of reflowed photoresist for micro structures (MSs) and self-masked dry etching method for subwavelength structures (SWSs), play an important role in enhancing the light extraction efficiency by reducing both the total internal reflection and the Fresnel reflection. HSs lead to an enhancement of optical output power of ~200% compared to the conventional VLEDs with flat surface as a result of reflection suppression and transmittance enhancement, without any serious degradation of electrical characteristics and a change of peak emission wavelength as function of injection current. Furthermore, optical simulations by ray-tracing and the rigorous coupled-wave analysis methods provide design guidelines for MSs and SWSs, respectively. © 2015 The Japan Society of Applied Physics

### 1. Introduction

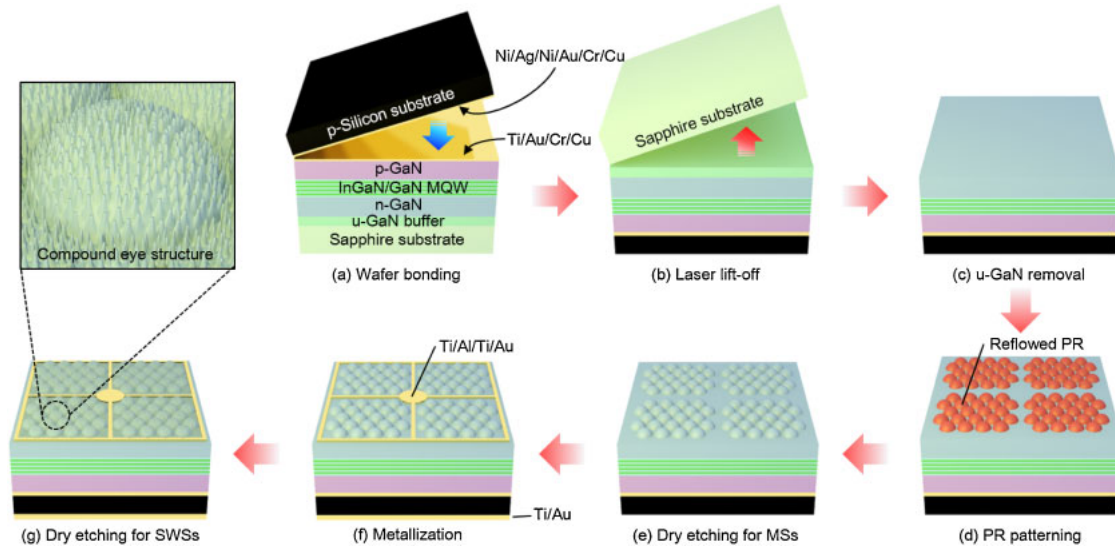
Hierarchical structures (HSs) have attracted significant interest in nature because of their unique properties, such as the antireflection behaviors of the compound eye of moths.<sup>1–3</sup> Compound eyes have various optical functions because they consist of micro structures (MSs) and subwavelength structures (SWSs). Among the various optical functions, one is the collecting or refracting of omnidirectional incident light according to geometric MSs.<sup>4,5</sup> Another is the broadband and omnidirectional antireflection properties of tapered SWSs which act as graded refractive index media.<sup>6–8</sup> These two functional structures can be utilized in a range of various optoelectronic devices such as solar cells, organic light-emitting diodes (LEDs), and inorganic LEDs to enhance the light absorption or extraction.<sup>9–14</sup> Especially, HSs are very powerful structures for enhancing the light extraction efficiency (LEE) of LEDs by reducing both the total internal reflection (TIR) loss and the Fresnel reflection (FR) loss caused by refractive index difference at the interface between GaN ( $n = 2.45$ ) and air ( $n = 1$ ). Previously, dry etched micropatterns, KOH wet etched for rough surface, and photochemical etching methods have been used to achieve improved light extraction, which in turn has resulted in significant increases in LEE in GaN-based VLEDs.<sup>15–22</sup> However, GaN-based VLEDs with HSs have not yet been reported despite their important functions.<sup>6</sup>

In this paper, we present GaN-based VLEDs with biomimetic HSs; these GaN-based VLEDs consist of cone-shaped MSs and tapered SWSs (nanotips), formed using the thermal reflow and self-masked dry etching (SMDE) processes,<sup>23,24</sup> respectively. SMDE process is quite simple method to fabricate nanostructure on surface of semiconductor materials because of mask free process. Also, optical simulations using the ray-tracing and rigorous coupled-wave analysis (RCWA) method were conducted to provide design guidelines for the MSs and SWSs, respectively.

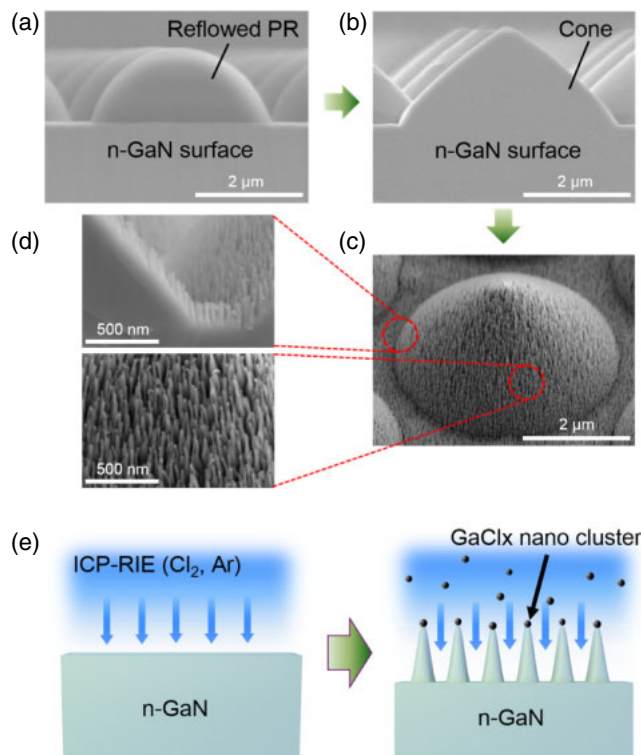
### 2. Experimental procedure

The GaN-based ( $\lambda = 530$  nm) epitaxial wafers used in this

study were grown on *c*-plane (0001) non-patterned sapphire ( $\text{Al}_2\text{O}_3$ ) substrates using a metal–organic chemical vapor deposition. The structure consists of 1- $\mu\text{m}$ -thick undoped GaN (u-GaN), 5- $\mu\text{m}$ -thick Si-doped n-type GaN (n-GaN), five period of InGaN/GaN multiple quantum wells, and 100-nm-thick Mg-doped p-type GaN (p-GaN). Figure 1 provides a schematic illustration of the process steps for the fabrication of HSs incorporated GaN-based VLEDs (HSs VLEDs). Using an e-beam evaporator, a Ni/Ag/Ni/Au (1/200/100/100 nm) metal layer was deposited on a p-GaN layer for an ohmic contact formation with high reflection.<sup>25</sup> After metal deposition, the sample was annealed using a rapid thermal annealing (RTA) system at 500 °C for 1 min in air ambient to form a p-type ohmic contact. A Cr/Cu (100/500 nm) metal layer was deposited onto a p-type ohmic and reflector layer for wafer bonding using the e-beam evaporator. Then, the Ni/Ag/Ni/Au/Cr/Cu metal deposited GaN-based wafer was bonded to the Ti/Au/Cr/Cu (100/100/100/500 nm) deposited 2-in. diameter p-Si(100) receptor for 30 min at 350 °C and 7 kgf/cm<sup>2</sup> using a wafer bonding system (Nano Sol-tech TPS-600-s). The sapphire substrate was removed using a 248 nm KrF excimer laser lift-off (LLO) system (QMC ELMS-1000).<sup>26–28</sup> The u-GaN was removed to expose the surface of n-GaN using inductive coupled plasma reactive ion etching (ICP-RIE). After square mesa (400 × 400  $\mu\text{m}^2$ ) patterning with photoresist (PR), ICP-RIE etching in  $\text{Cl}_2$  and Ar ambient was conducted for electric current isolation. For the fabrication of cone shape MSs on the surface of n-GaN, an array of hemispherical PR patterns with an approximate diameter of 3.5  $\mu\text{m}$  and height of 1.5  $\mu\text{m}$  was formed on the whole surface except for the n-contact area using conventional photolithography and thermal reflow process, as shown Fig. 2(a). Subsequently, pattern transfer process<sup>14</sup> was carried out to fabricate MSs on the surface of n-GaN with ICP-RIE at optimum conditions, i.e.,  $\text{SiCl}_4$  (7.5 sccm) and Ar (15 sccm) with RF power of 100 W, ICP power of 400 W, and pressure of 2 mTorr for 11 min as shown Fig. 2(b). Fabricated cone-shaped MSs have diameters of 4  $\mu\text{m}$  and heights of 2  $\mu\text{m}$  with a separation length of ~1  $\mu\text{m}$ . Before the SMDE process was used to form the



**Fig. 1.** (Color online) Schematic illustration of process steps for the fabrication of HSs incorporated GaN-based VLEDs using thermal reflow process and SMDE process.



**Fig. 2.** (Color online) SEM images of surface of n-GaN at each fabrication step for fabricating HSs on surface of n-GaN and schematic illustration of SMDE process. (a) Reflowed photoresist patterns on a surface of n-GaN. (b) Cone shape MSs patterned n-GaN through ICP-RIE. (c) HSs formed n-GaN using SMDE. (d) Magnification image of HSs as a partial position. (e) Schematic illustration of SMDE process using generated GaCl<sub>x</sub>.

SWSs on the MSs patterned surface of n-GaN, Cr/Au (100/3000 nm) and Ti/Au (100/3000 nm) metal layers were deposited on the n-contact area and back side of the p-Si(100) receptor, respectively. Finally, uniform and high-density SWSs were formed on the entire surface of the MSs formed n-GaN using a self-generated GaCl<sub>x</sub> nano cluster mask in an ICP-RIE chamber with optimum conditions,<sup>29,30</sup> i.e., Cl<sub>2</sub> (20 sccm) and Ar (2 sccm) with RF power of 30 W,

**Table I.** Elemental composition of surface of n-GaN as a function of etching time, determined by XPS analysis.

Element	Elements present (at. %)		
	2 min	4 min	6 min
Cl	1.91	1.98	2.99
Ga	18.8	19.01	19.28
N	62.93	60.71	55.55
Others (O and C)	16.37	17.26	20.44

ICP power of 900 W, and pressure of 2 mTorr for 7 min, as illustrated in Fig. 2(d). The elemental composition of the surface of the n-GaN was measured using X-ray photoelectron spectroscopy (XPS). Table I shows the rate of change of the elemental composition accordance to the etching time. The compositions of Cl and Ga were found to increase from 1.91 to 2.99% and from 18.8 to 19.28%, respectively. These results prove the existence of GaCl<sub>x</sub> on the surface of n-GaN. The fabricated SWSs have the a width of ~50 nm, height of 140–150 nm, and period of ~80 nm, as shown in Figs. 2(c) and 2(d). The samples were characterized using field-emission scanning electron microscopy (FE-SEM; Hitachi S-4700) with an operating voltage of 10 kV. In order to compare level of performance, GaN VLEDs with different surface morphology were simultaneously fabricated from the same LED epitaxial structure.

### 3. Results and discussion

Prior to fabricating the HSs, theoretical calculations of the TIR and FR were conducted in order to determine the shape of the MSs and the period of the SWSs, respectively. In the theoretical calculations, ray-tracing and RCWA methods were utilized separately due to the scale difference between the micro and subwavelength structures. The model for MSs used in this calculation has a diameter of 3 μm, a height of 1.5 μm, and separation length of 1 μm. We used four different geometries (i.e., cylinder, truncated cone, perfect cone, and hemisphere) in this simulation to find optimum structures, as shown at the left side of Fig. 3. Herein, the refractive index of

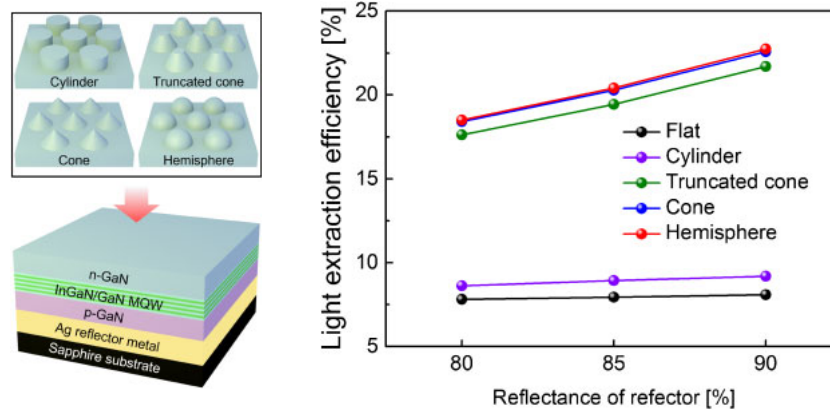


Fig. 3. (Color online) Calculated LEE as a function of geometry of the MSs. Image on left side indicates a calculation model.

n-GaN and that of the surrounding environment were defined as  $n = 2.45$  and 1, respectively. The absorbance of InGaN/GaN with 100 nm thickness was set at 0.125%/nm about 530 nm emission wavelength to reflect the actual and similar conditions. The LEE values of the VLEDs with various MSs as a function of the reflectance of the Ag reflector, are shown in the graph in Fig. 3.

The LEE of conventional VLEDs, as expected, was approximately ~8% due to light trapping phenomena caused by TIR; however, the cone shape and hemisphere shape MSs incorporated VLEDs showed values of 22.58 and 22.74% with reflectance values of 90% of the reflector because of the decrease of TIR. Therefore, cone and hemisphere shape MSs are expected to enhance the LEE of VLEDs. To further increase LEE by suppressing approximately 18% of the FR loss due to the refractive index difference between air and GaN, SWS simulation using RCWA method was performed to apply desirable SWSs on the surface of n-GaN. Figure 4 provides a contour plot of the calculated reflectance variation caused by FR as a function of the period of the SWSs and the incident wavelength (350–650 nm). Herein, SWSs had a 50 nm width and 150 nm height. The SWSs, which had a period of <90 nm, exhibited very low reflectance (~3%) within the 400–600 nm incident wavelength. Therefore, the period of the nanotip liked-SWSs should be shorter than ~90 nm in order to achieve very low reflectance.

In order to compare performances, the optical output power and forward voltage of VLEDs with different types of surface morphology were measured at normal direction and room temperature. To establish the reliability of the measurement results, randomly selected samples were measured 5 times and averaged. Figure 5(a) shows the light-current-voltage ( $L-I-V$ ) characteristics of the four fabricated types of VLEDs as a function of the continued bias current, simultaneously. Compared to flat VLEDs, all textured-VLEDs showed enhanced light-output power characteristics. MSs and SWSs VLEDs exhibited light-output power values of 15.19 and 6.49 mW/sr, respectively, at bias current of 300 mA, which values are significantly enhanced levels of light-output power compared to those of flat VLEDs (5.36 mW/sr). These results prove that MSs and SWSs can reduce the value of TIR and FR, respectively; the enhancement ratios of MSs and SWSs VLEDs were similar to those found in the calculation results. Among these results, the light-output power of HSs VLEDs showed its highest value

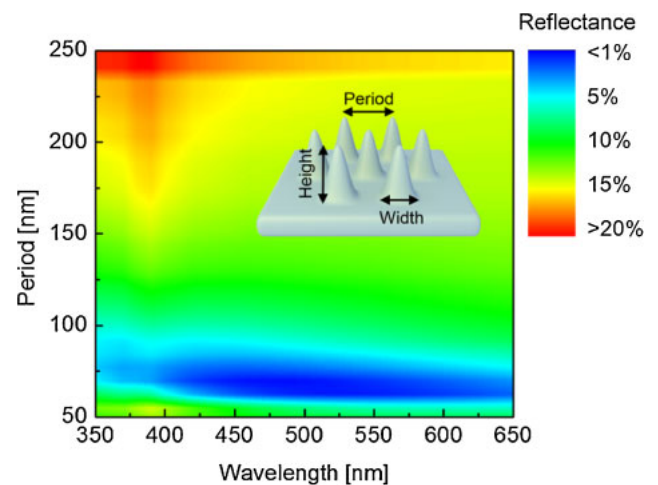


Fig. 4. (Color online) Contour plot of the calculated reflectance as a function of the period of SWSs and incident wavelength. In these calculations, the geometry of SWSs has 50 nm width and 150 nm height. Inset indicates a calculation model.

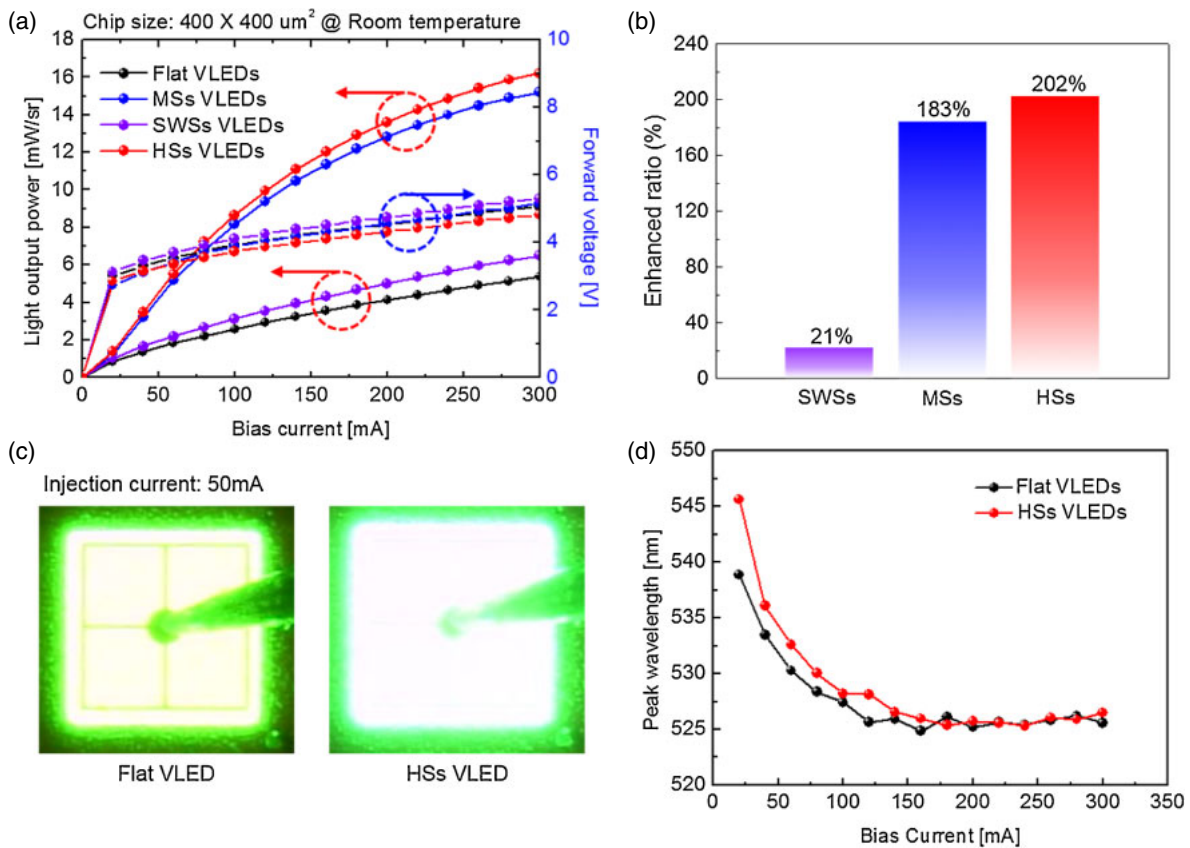
of 16.20 mW/sr at bias current of 300 mA, which results are caused by combining MSs and SWSs; Fig. 5(c) shows the brightness difference of flat and HSs VLEDs at injection current of 50 mA. The enhancement ratio of LEE of the HSs LED was an approximately 200% bias current of 300 mA without serious peak wavelength difference or degradation of the electrical characteristics, as shown in Figs. 5(a), 5(b), and 5(d). These results certainly show that HSs are suitable for use to enhance the LEE of VLEDs by reducing TIR and FR at the interface.

#### 4. Conclusions

In this work, we applied HSs on VLEDs to reduce both the value of TIR and FR by using low-cost fabrication methods such as thermal reflowed PR and SMDE. MSs and SWSs were fabricated based on theoretical calculations. The LEE of HSs VLEDs shows a 200% enhancement compared to that of flat VLEDs without serious degradation of the electrical characteristics or peak wavelength difference. Thus, our HSs are a promising solution for low-cost and high efficiency VLEDs.

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**Fig. 5.** (Color online) (a)  $L$ - $I$ - $V$  of conventional and textured-VLEDs as a function of bias current. (b) Enhancement ratio of SWSs, MSs, and HSs VLEDs. (c) Photograph images of the light emission from flat VLEDs and HSs VLEDs at injection current of 50 mA. (d) Peak wavelength spectra as a function of bias currents of 0–300 mA.

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