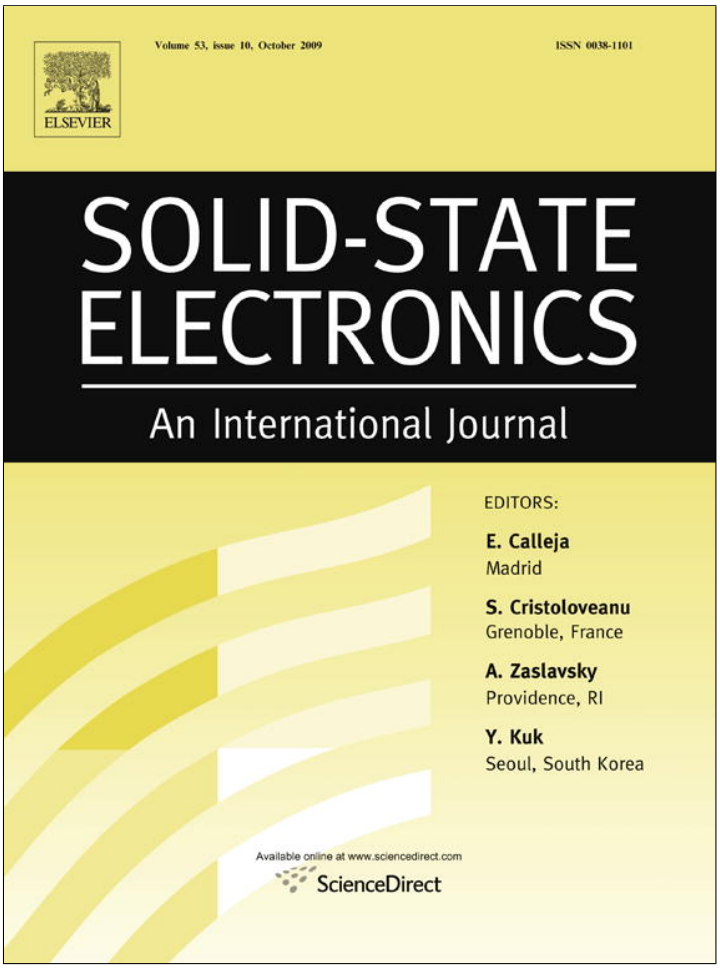

Solid-State Electronics 53 (2009) 1086–1091

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Thermal analysis of asymmetric intracavity-contacted oxide-aperture VCSELs for efficient heat dissipation

H.K. Lee [a], Y.M. Song [b], Y.T. Lee [b], J.S. Yu [a,*]

[a] Department of Electronic Engineering, Kyung Hee University, Yongin 446-701, Republic of Korea
[b] Department of Information and Communications, Gwangju Institute of Science and Technology, Gwangju 500-712, Republic of Korea

ARTICLE INFO

Article history:
Received 27 December 2008
Received in revised form 8 June 2009
Accepted 16 June 2009
Available online 26 July 2009

The review of this paper was arranged by Prof. E. Calleja

Keywords:
VCSELs
InGaAs/GaAs MQWs
Thermal analysis
Thermal resistance

ABSTRACT

The asymmetric intracavity-contacted oxide-aperture vertical-cavity surface-emitting lasers (VCSELs), operating at $\lambda \sim 980$ nm, with different oxide aperture diameters were fabricated and their thermal analysis was theoretically performed using a three-dimensional cylindrical heat dissipation model. The heat flux, temperature profile, and thermal resistance (R_{th}) of the devices were investigated by incorporating heat source values, obtained from experimentally measured results, into the thermal simulation. For the fabricated VCSELs with benzocyclobutene passivation layer, the R_{th} decreased from 4612 K/W to 1130 K/W as the oxide aperture diameter (D_a) increased from 8 μm to 16 μm and it increased significantly below 8 μm. The use of the thin substrate and the passivation layer with a high conductivity enhances the heat dissipation, allowing for a low R_{th}. Furthermore, thick Au layers on contact pads and top DBR in intracavity-contacted VCSEL structures help increase heat removal from the active region. For $D_a = 8$ μm and 16 μm, the VCSELs with SiN_x passivation layer, 5 μm thick extra Au layer, and 100 μm thick substrate indicate $R_{th} = 3050$ K/W and 778 K/W, respectively, leading to an improvement by >30% compared to the fabricated devices.

1. Introduction

The vertical-cavity surface-emitting laser (VCSEL) has become a standard light source for applications in high bit-rate data transmission and optical interconnection. The advantages, such as small size, low cost, low power consumption, and high speed modulation, make its cost-effective manufacturing possible. Recently, intracavity-contacted VCSELs, based on undoped distributed Bragg reflectors (DBR) mirrors and ring contacts, have exhibited improved performance over the conventional extracavity structure [1,2]. In the intracavity structure, current is injected into the active region without passing through either of the DBRs. This makes the contacts essentially coplanar with low series resistance as well as reduced parasitic capacitance, achieving high-speed operation [3,4]. Furthermore, additional process technologies, such as photonic crystals, microlens, and electroplated Au (or Cu), can be easily incorporated into the DBRs [5–7]. The use of asymmetric contact layout reduces an unfavorable current crowding effect at the oxide aperture region [8].

However, the thin-film VCSEL structure has usually poor thermal characteristics due to the relatively thick DBRs with low thermal conductivities and small current oxide apertures above and below the active region when compared to conventional edge emitting laser structure. The understanding of the thermal behavior of VCSELs is very important because the device performance, i.e., optical output power, threshold current, and modulation speed, was limited by thermal effects. Also, the thermal characteristics of VCSELs are expected to depend on their oxide aperture diameter (D_a). To gain a deep insight of the thermal behavior in the asymmetric intracavity-contacted VCSEL, therefore, the theoretical and systematical thermal analysis using a heat dissipation model is required. Eventually, the thermal analysis may lead to an optimum design of the device structure to improve the thermal management. In this paper, we fabricated asymmetric intracavity-contacted oxide-aperture VCSELs with different oxide aperture diameters to obtain experimentally the total heat power. Based on the experimental results, theoretical thermal analysis was systematically studied in various structure configurations using a three-dimensional (3D) cylindrical heat dissipation model to extract the thermal parameters such as internal temperature distribution, heat flux, and thermal resistance.

2. Device structure and thermal modeling

The $\lambda \sim 980$ nm asymmetric intracavity-contacted oxide-aperture VCSELs with $Al_{0.88}Ga_{0.12}As$ and GaAs DBR mirrors and benzocyclobutene (BCB) passivation layer for different oxide aperture

* Corresponding author. Tel.: +82 31 201 3820; fax: +82 31 206 2820.
E-mail address: jsyu@khu.ac.kr (J.S. Yu).

0038-1101/$ - see front matter © 2009 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2009.06.005

sizes were fabricated. The schematic diagram of the VCSEL structure is shown in Fig. 1.

The active region consisting of 1λ cavity with three periods of $In_{0.19}Ga_{0.81}As/GaAs$ (8.5 nm/10 nm) quantum wells (QWs) sandwiched by $Al_{0.3}Ga_{0.7}As$ cladding layers was grown on semi-insulating (SI) GaAs substrate by a molecular beam epitaxy. The cavity is bounded on each side by $Al_{0.98}Ga_{0.02}As$ layers, followed by p- and n-doped GaAs contact layers. The contact layers were optimized at $5/4\lambda$. The undoped top/bottom DBR mirrors consist of 22 and 30.5 pairs of undoped $Al_{0.88}Ga_{0.12}As/GaAs$ layers, respectively. The sample was processed into the first cylindrical mesa of 18 μm in diameter etched down to the p-GaAs contact layer and the second cylindrical mesa of 54 μm in diameter etched down to the n-GaAs contact layer. The $Al_{0.98}Ga_{0.02}As$ layers were selectively oxidized for lateral current confinement. The n-contact layer was etched for device isolation and BCB was coated on the sample for passivation and planarization. Pt/Ti/Pt/Au and Ni/Au/Ge/Ni/Au metals were formed on the p- and n-GaAs contact layers, respectively, by an e-beam evaporator. The device was mounted epilayer-up onto a copper heatsink and the measurements were performed under continuous-wave (CW) mode.

Thermal analysis based on the finite element method (FEM) was conducted to model the heat transport in the VCSEL structure using the commercial COMSOL software. The substrate thickness is about 300 μm. For devices with D_a = 4.5, 8, 10, 14, and 16 μm, the thermal calculation was carried out by the finite element method (FEM) simulation using a steady-state three-dimensional (3D) cylindrical heat dissipation model with physical parameters for their materials. The FEM simulation results for heat diffusion can be rather sensitive to the size of the simulation domain [9]. Here the simulations were performed for the large simulation domain of L_W = 300 μm in square size because the heat spreads out over much larger area compared to small hot spots of devices. The heat generated from the active region is transferred from the inside to the outside of the device by means of convection and radiation through the top electrodes and it is simultaneously transferred via the GaAs substrate to copper heatsink by conduction. The heat transfer is achieved mostly by conduction, where the device was in direct contact with the copper heatsink whose temperature was controlled by a thermoelectric cooler. The basic steady-state 3D heat transfer equations in cylindrical coordinates for thermal modeling are given as [10,11]

$$-\nabla\cdot(k\nabla T)=Q, \tag{1}$$

$$k\nabla T=h(T_{\text{inf}}-T)+\varepsilon\sigma(T_{\text{surr}}^4-T^4), \tag{2}$$

$$\nabla T=\frac{\partial T}{\partial r}\hat{r}+\frac{1}{r}\frac{\partial T}{\partial \phi}\hat{\phi}+\frac{\partial T}{\partial Z}\hat{z}, \tag{3}$$

where Q is the heat source density, k is the thermal conductivity, and T is the temperature. Also, h is the heat transfer coefficient, ε is the emissivity of the surface, σ is the Stefan–Boltzmann constant, T_{inf} is the far-enough (ambient) temperature, and T_{surr} is the surround temperature. We ignored the effect due to radiation since it is not the dominant heat transfer mechanism. In multilayer thin-film structures, the thermal conductivity is different compared to that of the bulk material due to the increased scattering by interface phonons [12]. The interface effects are caused partly by the thermal boundary resistance (TBR) associated with each interface, leading to the reduction in the thermal conductivity of the material [13–15]. The additional reduction in thermal conductivity by TBR might somewhat increase overall thermal resistance of the device. But there is still a shortage in studies on the TBR for a variety of interfaces. In this thermal analysis, the effective thermal conductivities with anisotropy were used for thin multilayers. The effective thermal conductivities in lateral and vertical directions are given by [16]

$$k_L=\frac{d_1k_1+d_2k_2}{d_1+d_2},\quad k_V=\frac{d_1+d_2}{d_1/k_1+d_2/k_2}, \tag{4}$$

where $k_1(k_2)$ and $d_1(d_2)$ is the thermal conductivity and thickness for layer 1 (layer 2), respectively. The DBR regions consist of nanometer-thick AlGaAs/GaAs multilayers. In this simulation, thus, the thermal conductivity could take on different values of k_L and k_V in the directions lateral and vertical to the layer structure, respectively, for more accurate calculations. In the QW region with three

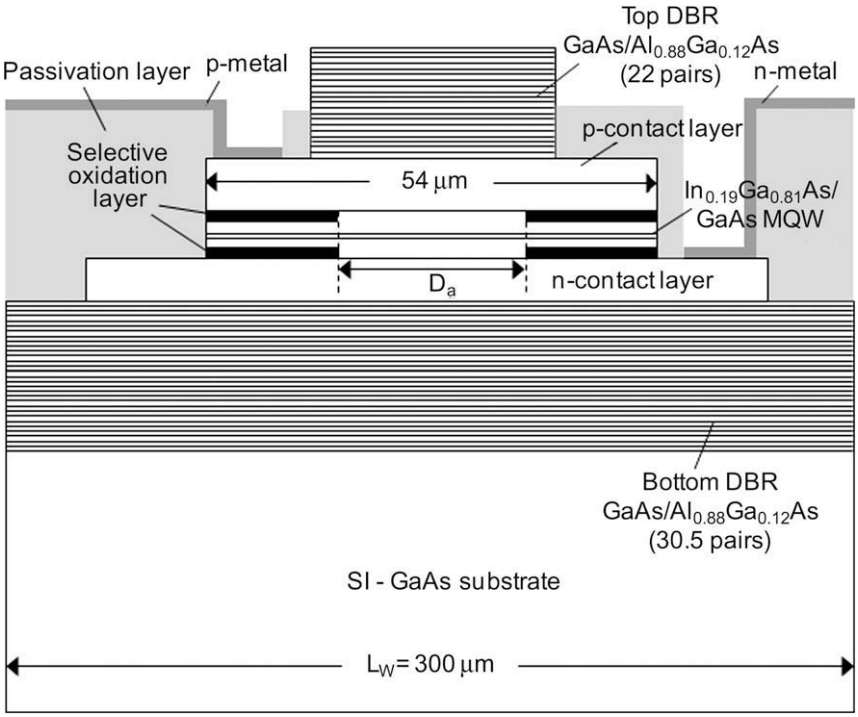

Fig. 1. Schematic diagram of $\lambda \sim 980$ nm asymmetric intracavity-contacted oxide-aperture VCSEL structure.

periods of nanometer-thick InGaAs/GaAs, there is additional reduction of the thermal conductivity caused by the acoustic phonon-boundary scattering and acoustic phonon confinement effects [17,18]. Thus, the effective thermal conductivity was also taken into account in the QW region. For all layers except the QW and DBR regions, isotropic thermal conductivity values ($k = k_L = k_V$) were taken into account. Table 1 shows the thermal conductivity for composite materials in intracavity-contacted oxide-aperture VCSELs mounted on the copper heatsink.

3. Results and discussion

Fig. 2a shows the CW light–current–voltage (L–I–V) curves of the fabricated VCSELs with different oxide aperture diameters. The scanning electron microscope (SEM) image of the fabricated device is also shown in the inset of Fig. 2. Devices exhibited optical output powers of 4.1 mW and 8 mW for $D_a = 4.5$ μm and 16 μm, respectively. The reduction of emission volume limits largely optical output power. The threshold current was increased from 0.5 mA at $D_a = 4.5$ μm to 2.2 mA at $D_a = 16$ μm. The heat sources are mainly distributed in the active region by nonradiative recombination and reabsorption of spontaneous emission of light, negligible Joule heating [19]. It is noted that the DBRs in intracavity-contacted VCSELs have no Joule heat generation because no current flow occurs through both top/bottom DBR mirrors. The heat source density, i.e., heat power generation per unit volume in 1λ cavity of active region, can be given by $Q = (V_{th}I_{th})/U$ at threshold, where V_{th} is the threshold voltage, I_{th} is the threshold current, and U is the volume of active region. The heat source density and series resistance as a function of oxide aperture diameter are shown in Fig. 2b. For $D_a = 16$ μm, the heat source density was approximately 4.3×10^{13} W/m^3 and it increased rapidly up to 1.39×10^{14} W/m^3 at $D_a = 4.5$ μm as the oxide aperture size of device became smaller. The series resistance (R_s) was increased from 120 Ω at $D_a = 16$ μm to 199 Ω at $D_a = 4.5$ μm with the decrease of oxide aperture diameter.

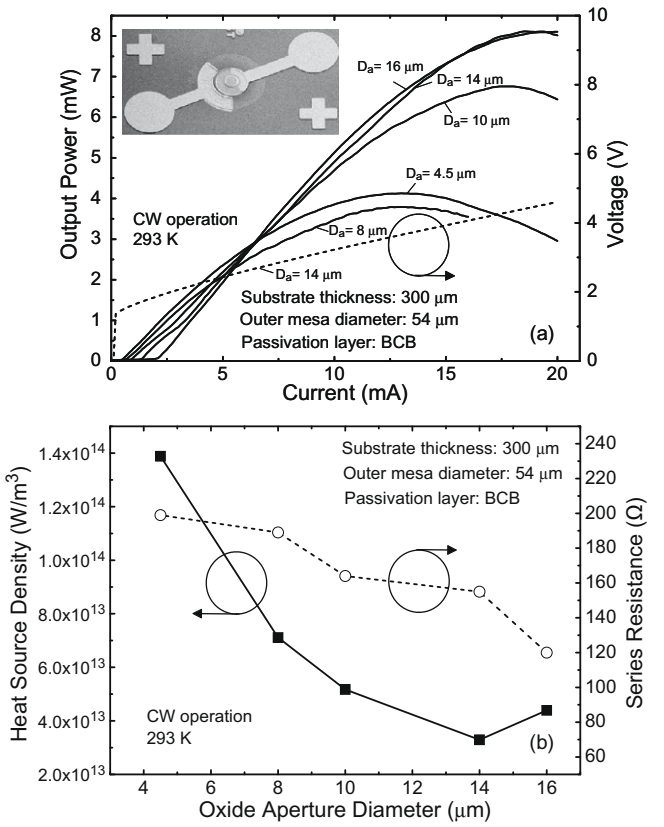

Fig. 2. (a) CW light–current–voltage (L–I–V) curves of the fabricated VCSELs with different oxide aperture diameters and (b) heat source density and series resistance as a function of oxide aperture diameter. The inset of Fig. 2a shows the SEM image of the fabricated device.

Fig. 3 shows (a) the heat flux and (b) the temperature distribution in lateral and vertical directions for an asymmetric intracavity-contacted oxide-aperture VCSEL. The heat flux is a vector quantity represented by the direction and magnitude of heat flow, indicating a fast heat flow path by long arrows. Large amounts of heat flow radially toward the substrate from heat sources by conduction because the device is contact with copper heatsink through bottom DBR and GaAs substrate. The heat was rapidly spread out over a wide area in the radial direction with long arrows. Partially, there was the heat extraction to the sides of the mesa through passivation layer and the top surface through top DBR as well as to Au contact pads in contact with air. The maximum internal temperature, which is caused by the heat generated inside the device, was raised up to 302.3 K in the active region for $D_a = 4.5$ μm of the VCSEL with BCB passivation layer when the heatsink was kept at 293 K.

Table 1
Thermal conductivity for composite materials in intracavity-contacted oxide-aperture VCSELs mounted on the copper heatsink [19–23].

	Material	Thermal conductivity (W/m K)	Thickness (nm)
p-Contact metal	Pt/Ti/Pt/Au	72/21.9/72/315	10/10/40/300
Top DBR	GaAs/$Al_{0.88}Ga_{0.12}As$	$k_L = 32.57$, $k_V = 29.26$	69.6/80.5 (22 pairs)
p$^+$-Metal contact layer	GaAs	44	487.2
Grading	$Al_{0.32}Ga_{0.68}As/Al_{0.43}Ga_{0.57}As/Al_{0.69}Ga_{0.31}As/Al_{0.88}Ga_{0.12}As$	14.55	4/4/4/4
Selective oxidation	Al_xO_y	0.7	49.5
	$Al_{0.98}Ga_{0.02}As$	58.43	
Grading	$Al_{0.88}Ga_{0.12}As/Al_{0.69}Ga_{0.31}As/Al_{0.43}Ga_{0.57}As$	15.45	4/4/4
Cladding layer	$Al_{0.32}Ga_{0.68}As$	11.87	106.1
3 MQW	$In_{0.19}Ga_{0.81}As$ (well)/GaAs (barrier)	$k_L = 29.52$, $k_V = 14.09$	15/8.5/10/8.5/10/8.5/15
Cladding layer	$Al_{0.32}Ga_{0.68}As$	11.87	106.1
Grading	$Al_{0.88}Ga_{0.12}As/Al_{0.69}Ga_{0.31}As/Al_{0.43}Ga_{0.57}As$	15.45	4/4/4
Selective oxidation	Al_xO_y	0.7	49.5
	$Al_{0.98}Ga_{0.02}As$	58.43	
Grading	$Al_{0.32}Ga_{0.68}As/Al_{0.43}Ga_{0.57}As/Al_{0.69}Ga_{0.31}As/Al_{0.88}Ga_{0.12}As$	14.55	4/4/4/4
n-Metal contact layer	GaAs	44	348
Bottom DBR	GaAs/$Al_{0.88}Ga_{0.12}As$	$k_L = 32.57$, $k_V = 29.26$	69.6/80.5 (30.5 pairs)
	$Al_{0.88}Ga_{0.12}As$	22.69	80.5
Substrate	GaAs	44	300,000
n-Contact metal	Ni/Au/Ge/Ni/Au	90.7/315/60/90.7/315	20/100/50/30/300

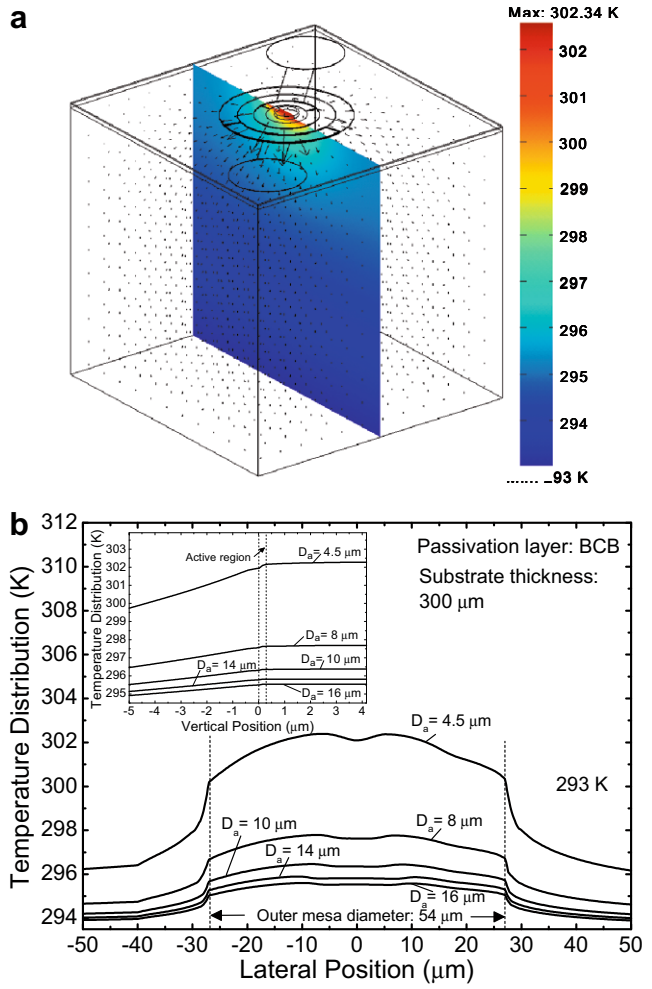

Fig. 3. (a) Heat flux and (b) temperature distribution in lateral and vertical directions for an asymmetric intracavity-contacted oxide-aperture VCSEL.

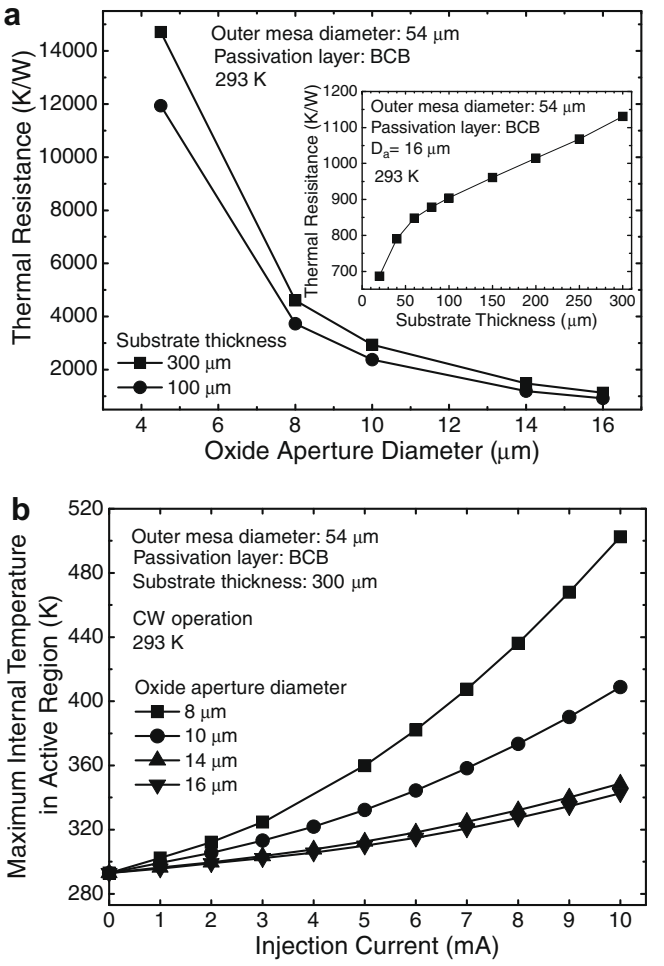

Fig. 4. (a) Thermal resistance at 293 K as a function of oxide aperture diameter for the VCSELs with substrate thicknesses of 100 μm and 300 μm and (b) maximum internal temperature in active region as a function of injection current for the VCSELs with D_a = 8, 10, 14, and 16 μm.

From the lateral temperature profiles in Fig. 3b, the heat generated in the active region was filed up within the outer mesa including active region because the oxide aperture layer has a relatively low thermal conductivity. Then, the heat was spread out laterally through the BCB passivation layer. The slightly low temperature distribution at the center of the outer mesa (i.e., lateral position = 0 μm) is originated from the enhancement of heat removal through the top DBR. We note that the heat source density becomes higher with decreasing oxide aperture size as shown in Fig. 2b. For the narrower oxide aperture, the selectively oxide layer adjacent to the heat generation region extends over the larger area and it prevents the generated heat from spreading out in the lateral direction. Thus, the temperature inside device increased as the oxide aperture diameter decreased. In the inset of Fig. 3b, the temperature gradient between the active region and substrate was displayed in the vertical direction, indicating a dominant heat removal toward the substrate, and it increased with the smaller aperture size.

Fig. 4a shows the thermal resistance at 293 K as a function of oxide aperture diameter for the VCSELs with substrate thicknesses of 100 μm and 300 μm. From the heat simulation with heat source densities, the thermal resistance of devices can be determined by $R_{th} = \Delta T/(V_{th}I_{th})$ at threshold, where ΔT is the maximum temperature deference between the active region and heatsink [24]. As expected, the thermal resistance increased as the oxide aperture diameter decreased. For the VCSEL with 300 μm thick substrate, the thermal resistance was lowered from R_{th} = 4612 K/W to R_{th} = 1130 K/W as the oxide aperture diameter increased from D_a = 8 μm to D_a = 16 μm and it increased significantly for D_a < 8 μm. The thermal resistance depends significantly on the substrate thickness. The VCSEL with a thin substrate of 100 μm indicated lower thermal resistance than the device with the substrate of 300 μm. This is ascribed to the short flow passage by removing layers in the heat flow path to heatsink. For the 100 μm thick substrate, the R_{th} value was reduced up to 3733 K/W at D_a = 8 μm and 917 K/W at D_a = 16 μm, thus leading to about 20% reduction of R_{th} compared to the 300 μm thick substrate. As shown in the inset of Fig. 4a, the thermal resistance was significantly reduced with the substrate thickness of <100 μm to low levels (e.g., 687 K/W at the substrate thickness of 20 μm) for D_a = 16 μm. This means that the bottom-emitting VCSELs with epi-layer-down bonding scheme and substrate removal is expected to have a lower thermal resistance due to the shorter heat transfer path length between the heat source and the heatsink. Fig. 4b shows the maximum internal temperature in active region as a function of injection current for the VCSELs with D_a = 8, 10, 14, and 16 μm. The internal temperature depending on injection current can be obtained from the equation given by [25]

$$T_{int} = T_{hs} + R_{th} \cdot (VI + R_s I^2 - P_{opt}), \quad (5)$$

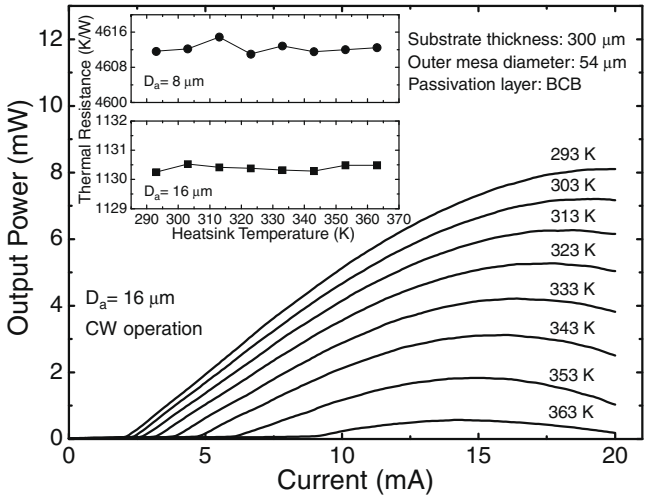

Fig. 5. Temperature dependent CW *I–V* curves of the fabricated VCSEL with $D_a = 16$ μm. The inset shows the calculated thermal resistance by FEM simulation using heat source densities obtained from the experimental data for $D_a = 8$ μm and $D_a = 16$ μm.

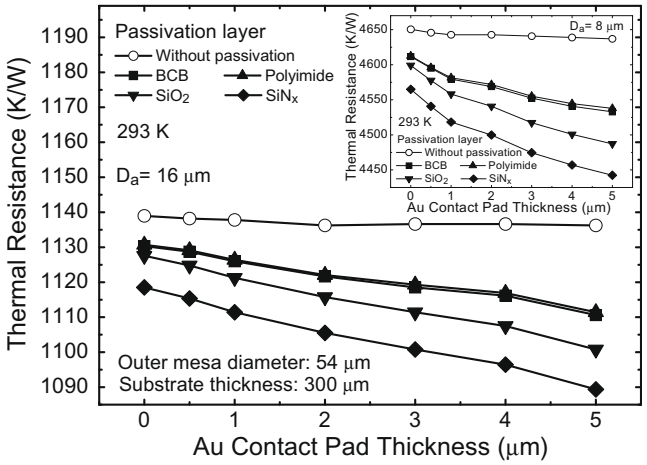

Fig. 6. Thermal resistance of the VCSELs with $D_a = 8$ μm and $D_a = 16$ μm as a function of Au contact pad thickness for various passivation layers.

where T_{int} is the internal temperature, T_{hs} is the heatsink temperature, V is the voltage, I is the injection current, and P_{opt} is the optical output power. The maximum internal temperature increased as the injection current increased. At an injection current of 10 mA, the ΔT was calculated as 50 K for $D_a = 16$ μm and as 209 K for $D_a = 8$ μm. For the narrow oxide aperture size, the temperature rise due to the internal heating was significant with injection current, causing the poor heat dissipation.

Fig. 5 shows the temperature dependent CW *I–V* curves of the fabricated VCSEL with $D_a = 16$ μm. As the temperature increased, the maximum output power decreased because of temperature-induced heating effects. The maximum output power was decreased up to 0.5 mW at 363 K and the threshold current was increased from 2.2 mW at 283 K to 9.1 mA at 363 K. The slope efficiency was reduced from 0.64 mW/mA to 0.1 mW/mA as the temperature was increased from 293 K to 263 K. The inset shows the calculated thermal resistance by FEM simulation using heat source densities obtained from the experimental data for $D_a = 8$ μm and $D_a = 16$ μm. The heat source density was increased from 7.1×10^{13} W/m^3 at 293 K to 2.1×10^{14} W/m^3 at 363 K and from 4.3×10^{13} W/m^3 at 293 K to 1.9×10^{14} W/m^3 at 363 K for $D_a = 8$ μm and $D_a = 16$ μm, respectively. At threshold, the thermal resistance of devices was kept almost constant, i.e., $R_{th} \sim 1130$ K/W at $D_a = 8$ μm and $R_{th} \sim 4612$ K/W at $D_a = 16$ μm, over a wide temperature range (293–363 K).

Fig. 6 shows the thermal resistance of the VCSELs with $D_a = 8$ μm and $D_a = 16$ μm as a function of Au contact pad thickness for various passivation layers. Without the passivation layer, the generated heat was transferred by convection into the air with a slow heat flow path. Thus, the thermal resistance was relatively high and it remained almost constant regardless of the Au contact pad thickness. The existence of passivation layer reduced the thermal resistance due to the enhanced heat removal by convection through it. Clearly, the use of a SiN_x passivation layer with a high thermal conductivity (i.e., $\kappa = 12$ W/m K) reduces the thermal resistance of device, allowing for effective heat dissipation. With passivation layers, the thermal resistance was decreased as the thickness of Au contact pad layer was increased due to the improved heat extraction from device to outside by the high conductive Au layer (i.e., $\kappa \sim 315$ W/m K). For $D_a = 16$ μm using the SiN_x passivation layer, the R_{th} value was decreased from 1140 K/W to 1089 K/W by using a 5 μm thick Au contact pad layer and it was reduced by about 4.5% compared to the device with no passivation layer. A similar trend was observed for the device with $D_a = 8$ μm.

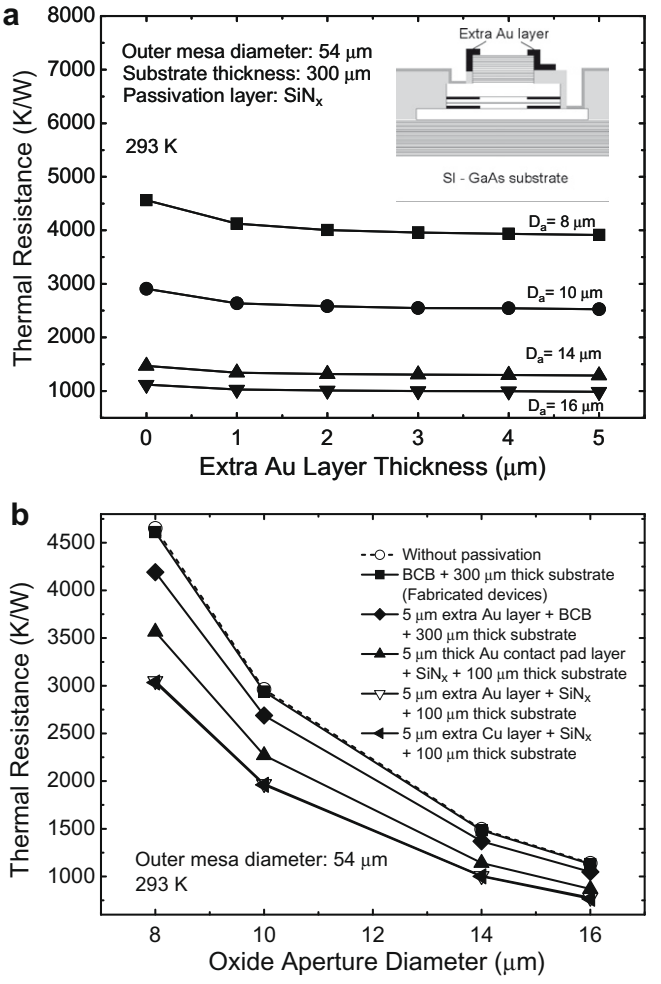

Fig. 7. (a) Thermal resistance as a function of extra Au layer thickness around the top DBR for VCSELs with different oxide aperture diameters and (b) thermal resistance as a function of oxide aperture diameter for different device structure schemes.

The heat dissipation capability also depends on the kind of passivation layer (i.e., its thermal conductivity).

Fig. 7a shows the thermal resistance as a function of extra Au layer thickness around the top DBR for VCSELs with different oxide aperture diameters. For efficient heat dissipation, the extra Au layer was incorporated on the surface of a top DBR mirror as shown in the inset of Fig. 6. As the extra Au layer became thicker, the internal temperature decreased, leading to the reduction in thermal resistance. It is evident that the use of extra Au layer helps dissipate easily more heat radially and upward into the air through it via top DBR. For the extra Au layer of 1 μm, the R_{th} value was reduced from 1119 K/W to 1028 K/W by 8.1% for D_a = 16 μm and it was reduced from 4565 K/W to 4125 K/W by 10% for D_a = 8 μm. However, it appeared to have little effect for extra Au layer of >1 μm due to the saturation in heat dissipation capability. The thermal resistance as a function of oxide aperture diameter for different device structure schemes is shown in Fig. 7b. The thermal conductance increases significantly for all these schemes as the oxide aperture diameter decreases. As shown in Fig. 7b, the additional extra Au layer of 5 μm on the fabricated device with D_a = 16 μm improved the R_{th} from 1130 K/W to 1047 K/W. For D_a = 16 μm, the VCSEL with SiN_x passivation layer, 5 μm thick extra Au layer, and 100 μm thick substrate indicates a low R_{th} = 778 K/W, leading to an improvement by >30% compared to the fabricated device. The device with no current path through the top DBR mirror, which acts as a heat generating source, may exhibit a low thermal resistance. The use of extra Cu layer ($\kappa \sim 398$ W/m K) instead of extra Au layer exhibited a reduction by only 5–21 K/W in R_{th}. It is found that the thermal resistance of asymmetric intracavity-contacted oxide-aperture VCSELs depends strongly on the oxide aperture size and it is reduced as the substrate becomes thinner. Furthermore, the use of passivation layer with high κ and extra Au (or Cu) layer further improves the thermal characteristics of the device due to the enhanced heat transfer capability.

4. Conclusions

We fabricated the 980 nm asymmetric intracavity-contacted oxide-aperture VCSELs with different oxide aperture sizes and the device characteristics were measured in the temperature range of 293–363 K. Using heat source densities from the experimental results for different oxide aperture diameters, the theoretical thermal analysis, including heat flux and temperature profile within the device, was carried out by FEM simulation, leading to the resultant thermal resistances. The thermal resistance increased significantly with a decrease in oxide aperture size, and it was also decreased as the substrate became thinner. For D_a = 16 μm, the R_{th} of 1130 K/W was obtained for the fabricated device with BCB passivation layer. The thermal resistance of devices remained almost constant over the temperature range of 293–363 K. The R_{th} of the device depends on the thermal conductivity of passivation layer. The use of thick Au layer on contact pads and extra Au layer on top DBR helps spread effectively the generated heat outside the device. Compared to the fabricated VCSELs, the devices with SiN_x passivation layer, 5 μm thick extra Au layer, and 100 μm thick substrate improved above 30% in the R_{th}, exhibiting a R_{th} = 778 K/W at D_a = 16 μm. These results are expected to provide a better understanding of the thermal behavior in asymmetric intracavity-contacted VCSELs to improve the device performance.

Acknowledgement

This work was supported by the IT R&D program of MKE/IITA (2007-F-045-02, Development of the projection input/output optical platform for realistic portable devices).

References

[1] MacDougal MH, Geske J, Lin CK, Bond AE, Dapkus PD. Thermal impedance of VCSEL's with AlO_x–GaAs DBR's. IEEE Photon Technol Lett 1998;10:15–7.
[2] Lysak VV, Chang KS, Lee YT. Top mirror optimization of high-speed intracavity-contacted oxide-confined vertical-cavity surface-emitting lasers. J Optoelectron Adv Mater 2006;8:355–8.
[3] Dang G, Hobson WS, Chirovsky LMF, Lopata J, Tayahi M, Chu SNG, et al. High-speed modulation of 850-nm intracavity contacted shallow implant-apertured vertical-cavity surface-emitting lasers. IEEE Photon Technol Lett 2001;13:924–6.
[4] Scott JW, Thibeault BJ, Young DB, Coldren LA, Peters FH. High efficiency submilliamp vertical cavity lasers with intracavity contacts. IEEE Photon Technol Lett 1994;6:678–80.
[5] Leisher PO, Danner AJ, Choquette KD. Single-mode 1.3-μm photonic crystal vertical-cavity surface-emitting laser. IEEE Photon Technol Lett 2006;18:2156–8.
[6] Chang KS, Song YM, Lee YT. Self-aligned microlens-integrated vertical-cavity surface-emitting lasers. IEEE Photon Technol Lett 2006;18:2203–5.
[7] AL-Omari AN, Carely GP, Hallstein S, Watson JP, Dang G, Lear KL. Low thermal resistance high-speed top emitting 980-nm VCSELs. IEEE Photon Technol Lett 2006;18:1225–7.
[8] Krishnamoorthy AV, Chirovsky LMF, Hobson WS, Lopata J, Shah J, Rozier R, et al. Small-signal characteristics of bottom-emitting intracavity contacted VCSEL's. IEEE Photon Technol Lett 2000;12:609–11.
[9] Turin VO, Balandin AA. Electrothermal simulation of the self-heating effects in GaN-based field-effect transistors. J Appl Phys 2006;100:054501.
[10] Zhu C, Zhang Y, Li A, Tian Z. Analysis of key parameters affecting the thermal behavior and performance of quantum cascade lasers. J Appl Phys 2006;100:053105.
[11] Mehandru R, Dang G, Kim S, Ren F, Hobson WS, Lopata J, et al. Finite difference analysis of thermal characteristics of CW operation 850 nm lateral current injection and implant-apertured VCSEL with flip–chip bonding design. Solid State Electron 2002;46:699–704.
[12] Cahill DG, Ford WK, Goodson KE, Mahan GD, Majumdar A, Maris H, et al. Nanoscale thermal transport. J Appl Phys 2003;93:793–818.
[13] Sarua A, Ji H, Hilton KP, Wallis DJ, Uren MJ, Martin T, et al. Thermal boundary resistance between GaN and substrate in AlGaN/GaN electronic devices. IEEE Trans Electron Dev 2007;54:3152–8.
[14] Quintana JA, Viejo JR. Interfacial effects on the thermal conductivity of a-Ge thin films grown on Si substrates. J Appl Phys 2008;104:074903.
[15] Mackenzie R, Lim JJ, Bull S, Sujecki S, Rakins EC. Inclusion of thermal boundary resistance in the simulation of high-power 980 nm ridge waveguide lasers. Opt Quant Electron 2008;40:373–7.
[16] Osinski M, Nakwaski W. Effective thermal conductivity analysis of 1.55 μm InGaAsP/InP vertical-cavity top-surface-emitting microlasers. Electron Lett 1993;29:1015–6.
[17] Balandin A, Wang KL. Significant decrease of the lattice thermal conductivity due to phonon confinement in a free-standing semiconductor quantum well. Phys Rev B 1998;58:1544–9.
[18] Khitun A, Balandin A, Liu JL, Wang KL. In-plane lattice thermal conductivity of a quantum-dot superlattice. J Appl Phys 2000;88:696–9.
[19] Ouchi T. Thermal analysis of thin-film vertical-cavity surface-emitting lasers using finite element method. Jpn J Appl Phys 2002;41:5181–6.
[20] Nakwaski W. Thermal conductivity of binary, ternary, and quaternary III–V compounds. J Appl Phys 1988;64:159–66.
[21] Guden M, Piprek J. Material parameters of quaternary III–V semiconductors for multilayer mirrors at 1.5 μm wavelength. Model Simulat Mater Sci Eng 1996;4:349–57.
[22] Piskorski L, Sarzała RP, Nakwaski W. Self-consistent model of 650 nm GaInP/AlGaInP quantum-well vertical-cavity surface-emitting diode lasers. Semicond Sci Technol 2007;22:593–600.
[23] Hu C, Kiene M, Ho PS. Thermal conductivity and interfacial thermal resistance of polymeric low k films. Appl Phys Lett 2001;79:4121–3.
[24] Lee HK, Chung KS, Yu JS. Thermal analysis of InP-based quantum cascade lasers for efficient heat dissipation. Appl Phys B: Lasers Opt 2008;93:779–86.
[25] Rossbach R, Ballmann T, Butendeich R, Schweizer H, Scholz F, Jetter M. Red VCSEL for high-temperature applications. J Cryst Growth 2004;272:549–54.