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LOCAL SCIENTIFIC SECRETARIAT

Manuela Tetzlaff (TU Dresden, DE)

ORGANIZING SECRETARIAT

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DRESDEN - THE CAPITAL OF SAXONY, GERMANY

With about 550.000 inhabitants, Dresden is the capital of the Free State of Saxony and well known as the semiconductor capital of Germany as well as one of the leading semiconductor sites in Europe. The region therefore is often referred to as Silicon Saxony. In Saxony approximately 2.100 companies with more than 51.000 employees develop, manufacture, and promote integrated circuits, serve as materials and equipment suppliers to the chip industry, produce and distribute electronic products and systems based on integrated circuits, or develop and promote software. Saxony has an excellent research environment with 4 universities, 5 universities of applied sciences, 9 Fraunhofer Institutes, 4 Leibniz Institutes, 2 Max-Planck-Institutes and one Helmholtz Center.

The University of Technology in Dresden (TU Dresden), is one of the excellence universities of Germany, with more than 35.000 students. In 2006, TU Dresden created NaMLab, a research oriented daughter company and associated institute focused on research in materials for electron devices. Since 2011, the excellence cluster center for advancing electronics Dresden (cfaed) has bundled the TU Dresden research on electronics for the post-Moore era. The large research and development clusters Cool-Silicon and FAST connect industrial R&D to research organizations. Beyond science and technology Dresden is known for its architectural sites and arts. “Florence on the Elbe”, as Dresden is sometimes called, has many exciting faces, e.g.: the Frauenkirche and the Old Masters, the Semperoper, the Blue Wonder and the Green Vault, the picturesque banks of the Elbe and the popular Wilhelminian district, the Saxon State Orchestra and the International Dixieland Festival, the baroque Old Town and the modern city center, the Garden Suburb and the cultural metropolis.

CALL FOR PAPERS

WWW.ESSCIRC-ESSDERC2018.ORG

Organizers — TECHNISCHE UNIVERSITÄT DRESDEN; namlab nanoelectronic materials laboratory

Technical Co-Sponsorship — IEEE

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GENERAL PURPOSE OF THE CONFERENCE

The aim of **ESSDERC** and **ESSCIRC** is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The level of integration for system-on-chip design is rapidly increasing. This is made available by advances in semiconductor technology. Therefore, more than ever before, a deeper interaction among technologists, device experts, IC designers and system designers is necessary. While keeping separate Technical Program Committees, **ESSDERC** and **ESSCIRC** are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions, regardless to which conference they belong.

CONFERENCE HIGHLIGHTS

- 3 joint keynote presentations
- 3 **ESSDERC** keynote presentations
- 3 **ESSCIRC** keynote presentations
- Invited papers with overall coverage of all aspects of advanced devices and circuits
- Special Focus Sessions on
  - FDSOI
  - Power Electronics
- Presentation of IEEE and **ESSDERC**/**ESSCIRC** Awards
- **ESSDERC**/**ESSCIRC** Gala Dinner on Wednesday, September 5, 2018
- Tutorials
  - The Future of Mobility: Reliability, Readiness & Robustness of Integrated Circuits
    - Chapter 1: EOS & ESD
    - Chapter 2: Reliability & Readiness of IC's
    - Chapter 3: Mobility & Sensing
  - IC Design for Automotive
  - Ultra-Low Power Sensors for Condition Monitoring
- Workshops

The venue of the conference events, including workshops and tutorials, will be at the campus of TU Dresden close to the city center of Dresden.

The working language of the conference is English.

CONFERENCE TOPICS

Although not limited, papers are solicited for the following main topics:

ESSDERC

CMOS Devices and Technology

CMOS scaling, Novel MOS device architectures; Circuit/device interaction and co-optimization; High-mobility channel devices; CMOS front-end or back-end processes; Interconnects; Integration of RF or photonic devices; 3D integration. Front-end and back-end manufacturing processes; 3D integration and wafer-level packaging; Reliability and characterization of materials, processes and devices; Advanced interconnects; ESD, latch-up, soft errors, noise and mismatch behavior, hot carrier effects, bias temperature instabilities, and EMI; Defect monitoring and control; Metrology; Test structures and methodologies; Manufacturing yield modeling, analysis and testing.

Opto-, Power and Microwave Devices

New device or process architectures; New phenomena and performance improvement of optoelectronic, high voltage, smart power, IGBT, microwave devices; Passive devices, antennas and filters (including Si, Ge, SiC, GaN); Optoelectronic devices including sensors, LEDs, semiconductor lasers; Photovoltaic devices; Studies of high temperature operation; IC cooling and packaging aspects. Reliability and characterization of materials, processes and devices.

Physical Modeling of Materials and Devices

Numerical, analytical and statistical modeling and simulation of electronic, optical or hybrid devices, the interconnect, isolation and 2D or 3D integration; Aspects of materials, fabrication processes and devices e.g. advanced physical phenomena (quantum mechanical and non-stationary transport phenomena, ballistic transport, …); Mechanical or electro-thermal modeling and simulation; DfM. Reliability of materials and devices.

Compact Modeling of Devices and Circuits

Compact/SPICE modeling of electronic, optical, organic, and hybrid devices and their IC implementation and interconnection. Topics include compact/SPICE models and their Verilog-A standardization of the semiconductor devices (including Bio/Med sensors, MEMS, Microwave, RF, High voltage and Power), parameter extraction, compact models for emerging technologies and novel devices, performance evaluation, reliability, variability, and open source benchmarking/implementation methodologies. Modeling of interactions between process, device, and circuit design as well as Foundry/Fabless Interface Strategies.

Memory Devices and Technology

Embedded and stand-alone memories; DRAM, FeRAM, MRAM, ReRAM, PCRAM, Flash, Nanocrystal and single/few-electron memories, Organic memories, NEMS-based devices, Selectors; Novel memory cell concepts and architectures, covering device physics, reliability, process integration and manufacturability issues and including 3D NAND Flash, crosspoint arrays, and 3D systems integration; Devices and concepts for neuromorphic computing, memory-enabled logic and security applications.

Sensor Devices and Technology

Design, fabrication, modeling, reliability, packaging and smart systems integration of actuators (discrete SoC, SiP, or heterogenous 3D integration); MEMS, NEMS, optical, chemical or biological sensors; Display technologies; High-speed imagers; TFTs; Organic and flexible substrate electronics.

Emerging non-CMOS Devices and Technologies

Novel non-CMOS materials, processes and devices, (carbon-nanotubes, nanowires and nanoparticles, 2D materials, graphene, metal oxides, …) for electronic, optoelectronic, sensor & actuator applications; Reliability and characterization of materials, processes and devices; Molecular and quantum devices; Nanophotonics, plasmonics, spintronics, self-assembling methods; Energy harvesters; High frequency digital and analog devices including THz; New high-mobility channels (strained Si, Ge, SiGe).

ESSCIRC

Analog

OP-Amps and instrumentation amplifiers; CT and DT filters; SC circuits, Comparators; Voltage and current references; high voltage circuits; Nonlinear analog circuits; Digitally assisted analog circuits.

Data Converters

Nyquist-rate and oversampling A/D and D/A converters; Sample-hold circuits; Time-to-digital converters; ADC and DAC calibration/error correction circuits.

RF and mm-Wave

RF/IF building blocks like LNAs, mixers, power amplifiers, IF amplifiers; Power detectors; Subsystems for RF, mm-wave and THz design.

Frequency Generation

Modulators/demodulators; VCOs; PLLs; DLLs; Frequency synthesizers; Frequency dividers; Integrated passive components.

Wireless and Wireline Systems

Receivers/transmitters/transceivers for wireless/wireline systems Gigabit serial links; Clock and data recovery; Equalization; Advanced modulation systems; Base station and handset applications; TV/radio/satellite receivers and transmitters; Radars.

Sensors, Imager and Biomedical

Sensor subsystems and interfaces; Accelerometers; Temperature sensing; Imaging and smart imaging chips; AMOLED; MEMs subsystems; RF MEMs; Implantable electronic ICs; Biomedical imagers; Bio-MEMs integrated systems; Lab-on-chip; Organic LED and liquid-crystal-display interface circuits; Flat panel and projection display.

Digital, Security and Memory

Techniques for energy efficient and high performance digital circuits; I/O and inter-chip communication; Reconfigurable digital circuits; Security and encryption circuits; Clocking; Arithmetic building blocks; Memories; Microprocessors; DSPs; Memory interfacing; Bus interfacing; Many core and multi-rate ICs; 3D integration.

Power Management

Energy transducers; Power regulators; DC-DC converters; Energy-scavenging circuits; LDOs Boost-buck-converters; LED and gate drivers; Sequencers and supervisors; Green circuits.

PAPER SUBMISSION

Manuscript guidelines as well as instructions on how to submit electronically will be available on the conference website.
Papers must not exceed four A4 pages with all illustrations and references included.
All submissions must be received by 3 April, 2018.

Papers submitted for review must clearly state:
- The purpose of the work
- How and to what extent it advances the state-of-the-art
- Specific results and their impact

Only work that has not been previously published or submitted elsewhere will be considered.
Submission of a paper for review and subsequent acceptance is considered as a commitment that the work will not be publicly available prior to the conference.

After selection of papers, the authors will be informed about the decision of the Technical Program Committee by e-mail by May 18th, 2018.

At the same time, the complete program will be published on the conference website.
An oral presentation will be given at the Conference for each accepted paper. No-shows will result in the exclusion of the papers from the Conference Proceedings and the IEEE Xplore Digital Library.

For each paper independently, at least one co-author is required to register for the Conference (one registration-one paper policy).

Registration fees and deadlines will be available on the conference website.