Design and Implementation of Nowlin Circuit

INTRODUCTION

The following paper describes a small portion of hardware used in discriminator circuit. Discriminator circuit is a part of HINP (Heavy Ion Nuclear Physics) Integrated circuit called DISC16C, a 16 channels discriminator. Discriminator is used to mark the arrival time of an input pulse, which is independent of pulse amplitude and risetime. To make it independent of these, an attenuated version of the input is subtracted from a delayed version of input waveform and the time at which the difference between the two signals is equal to zero is used to mark the pulse arrival time.

There are two major factors related to this discriminator circuit and effect it's working. They are time walk t_w and time jitter $\sigma_{t.}$ Time walk is used to describe the systematic variation in the rising edge of the discriminator output signal as a function of pulse height. Jitter is electronics noise due to the various electronic components.

CIRCUIT DESIGN

Nowlin circuit consist of two resistances R_1 (R_{1A} & R_{1B}) & R_2 and two capacitors C_1 and $C_{2.}$ Capacitor C_1 along with R_{1A} & R_{1B} forms a high pass filter which is also called a fast shaper. Output of fast shaper is given to the leading-edge output which acts as an input to the leading-edge discriminator circuit. A part of fast shaper also goes to the zero-cross discriminator. This part is attenuated pulse which is defined as a fraction $K = \frac{R1A}{R1A+R1B}$ becomes an inverting input of zero-cross discriminator.

A delayed pulse along with this inverted input also goes to the zero-cross discriminator. This pulse is taken from between R_2 and $C_{2.}$ This zero-cross output is independent of input pulse amplitude.

The design requirement is to accommodate an input pulse having rise time of 25ns. To maintain that, delay circuit should be design such that $Ƭ_2 = C_2 * R_2$, where $Ƭ_2$ = 25ns. We can assume either C_1 or R_2.

Let's assume C_2 = 8 pf, then we will get R_2 is 3.125K Ω. Once we have the value of R_2, we can assume value of R_1. Since $Ƭ_1 >> Ƭ_2$ to produce maximum slew rate. We should select the value of such that $R_1 >> R_2$. But at the same time, we must ensure a sufficiently large amount of underdrive. To maintain both, suspected value of C_1 should be 3-5 times larger than C_2.

By using trial and error method we can figure out the value of R_{1A} and R_{1B} which is around 7 K Ω and 3.5 KΩ. Ratio of R_{1A} and R_{1B} should be kept as 2:1. To maintain matching throughout the design we can select the values as 6.25K and 3.12K. Similarly, to maintain a decent matching we can take C_1 as 28 pf. This splits the capacitors in 7 equal parts of 4 pf and C_2 can be split into two equal parts of 4pf each.

Time Jitter σ_j of the circuit can be calculated as the ration of noise and slew rate. Noise and slew rate can be calculated using simulation results done in cadence virtuoso.

$$\sigma_j = \frac{\sigma v}{SR}$$

Electronic noise σ_v associated with Nowlin circuit can be expressed as $\sqrt{\frac{kT}{C2}}$. One can clearly see that noise can be decreased by increasing the value of C_2.

DESIGN SUMMARY

Design can be implemented using three resistances R_{1A}, R_{1B} & R_2 of values 6.25KΩ, 3.125KΩ & 3.125k Ω respectively along with two capacitance C_1 and C_2 with values of 28pf and 8 pf respectively.

Circuit has one input which is driven by the exponential voltage source and three inputs ZC_OUTM, ZC_OUTP and LE_OUTP. LE_OUTP is the output from fast shaper, ZC_OUTP is the delayed output and ZC_OUTM is the inverted output of the pulse.

A complete top to bottom design hierarchy is shown in the figures below:

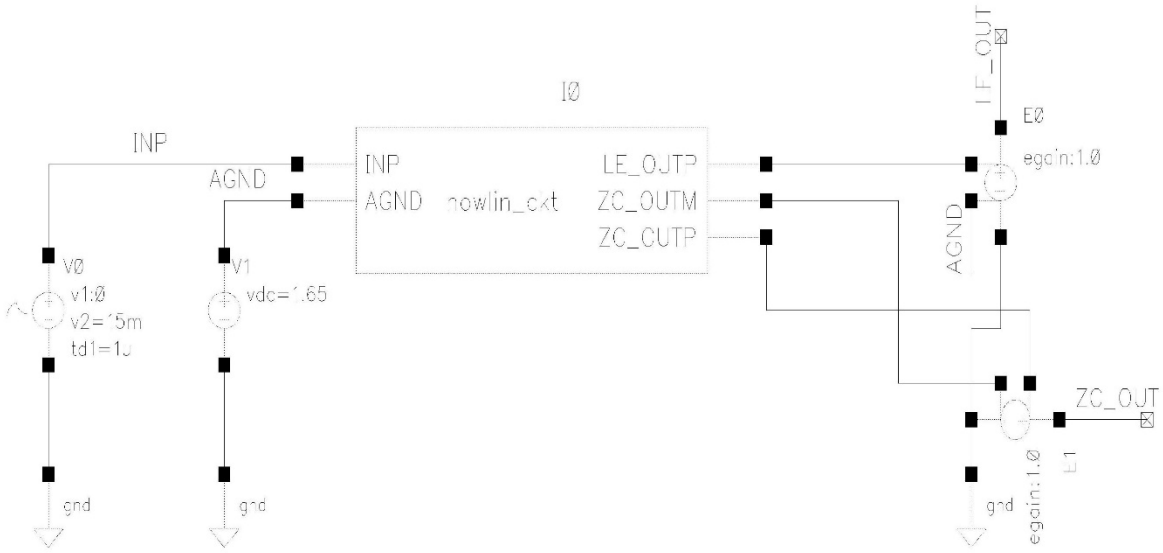

Figure 1. Nowlin Circuit test bench.

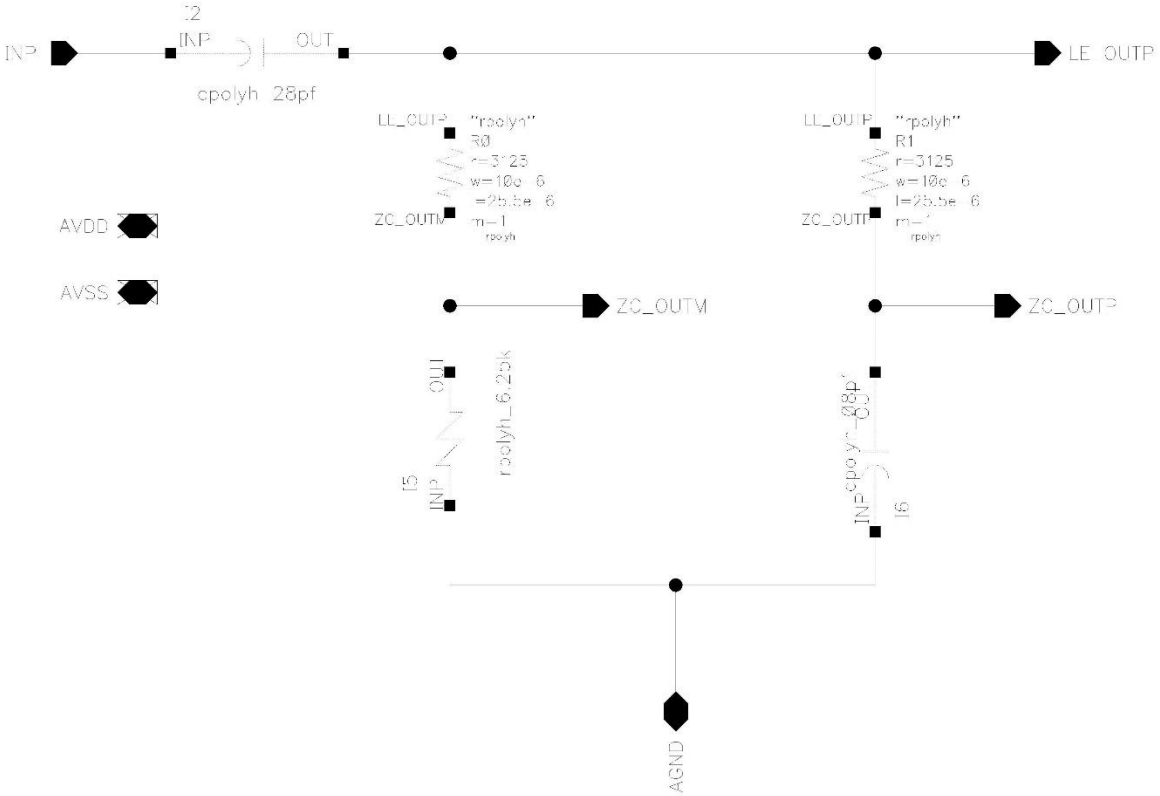

Figure 2. Nowlin Circuit Schematic.

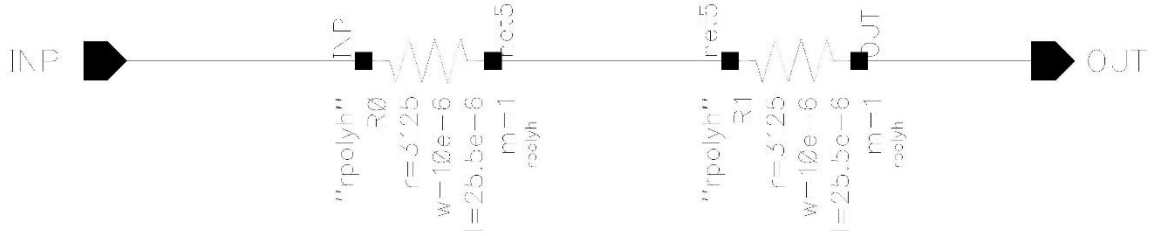

Figure 3. Resistance R_{1A} schematic using rpolyh.

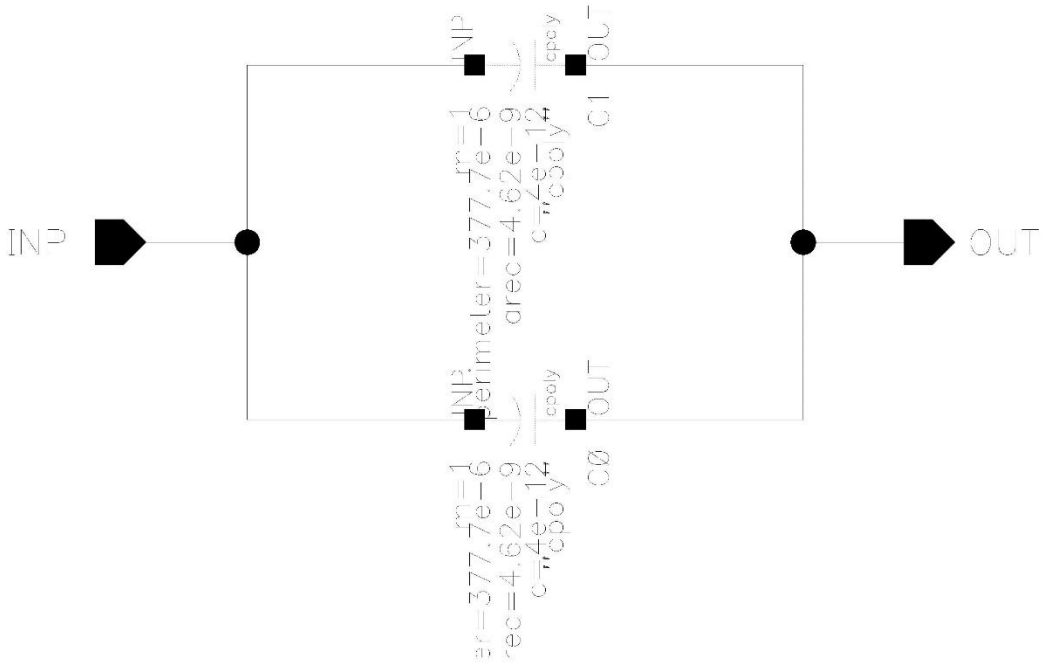

Figure 4. Capacitance C_2 schematic using cpoly.

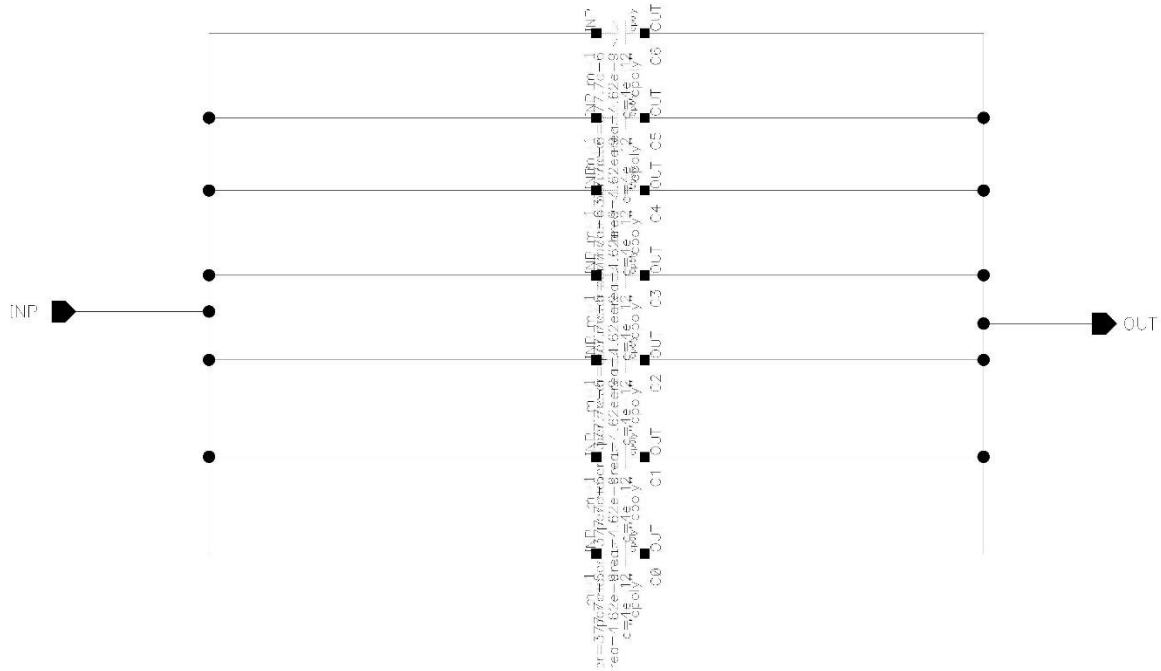

Figure 5. Capacitance C_1 schematic using cpoly.

DESIGN OUTCOMES

The Nowlin circuit can be analyzed using transient analysis and noise analysis. Using transient analysis, one can find out the slew rate produced by the circuit. Same way we can analyze the electronic noise produced by the various components in the circuit.

1. Slew rate calculation:

   Slew rate can be calculated using transient analysis results. It can be calculated taking difference between one point down zero cross and one point above zero cross. This difference can be divided by the distance between these two points which gives us the slew rate. Figure 6 shows the calculation of slew rate.

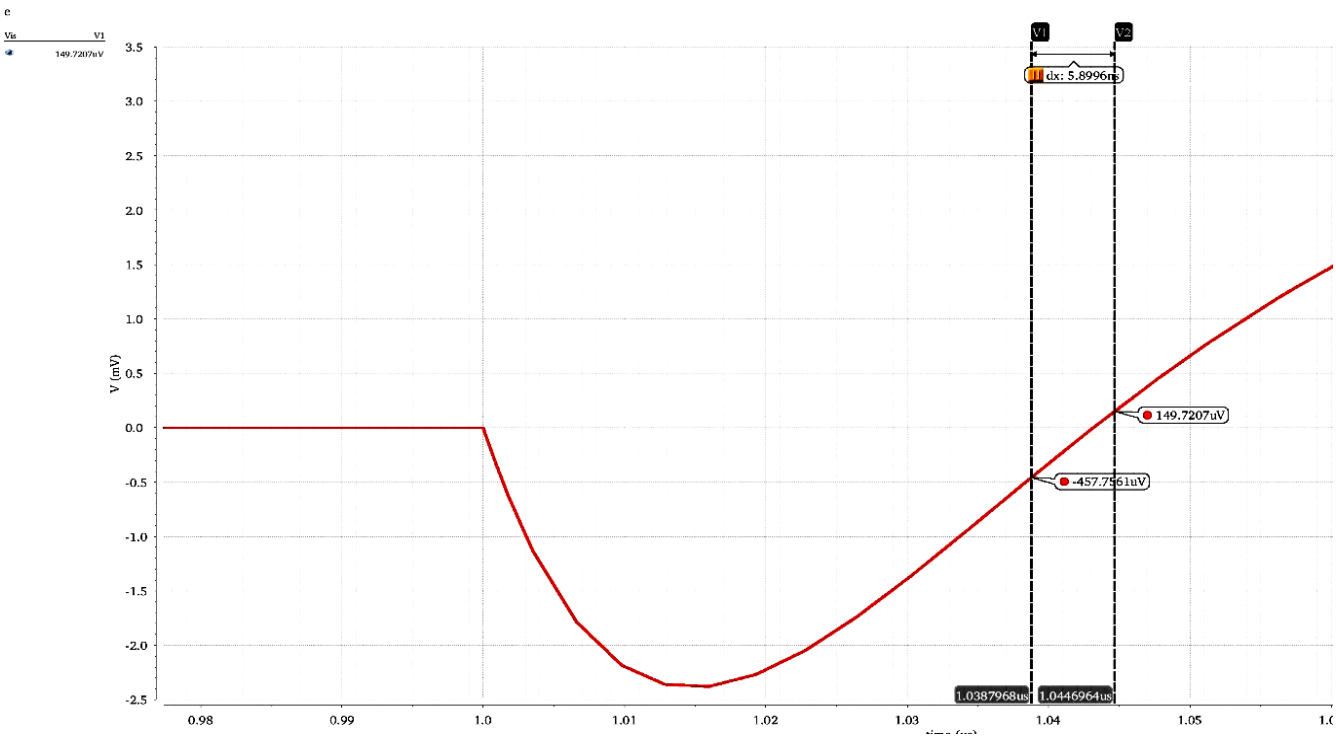

Figure 6. Slew rate calculation from ZC_OUT transient analysis. (closeup view)

From the graph one can see

$$\text{SR} = \frac{149.720\mu V - (-457.756\mu V)}{5.899\ ns} = 103\text{x}10^3\ \text{V/Sec}$$

Similarly, we can also run the noise analysis for a frequency range between 1 Hz to 10M Hz.

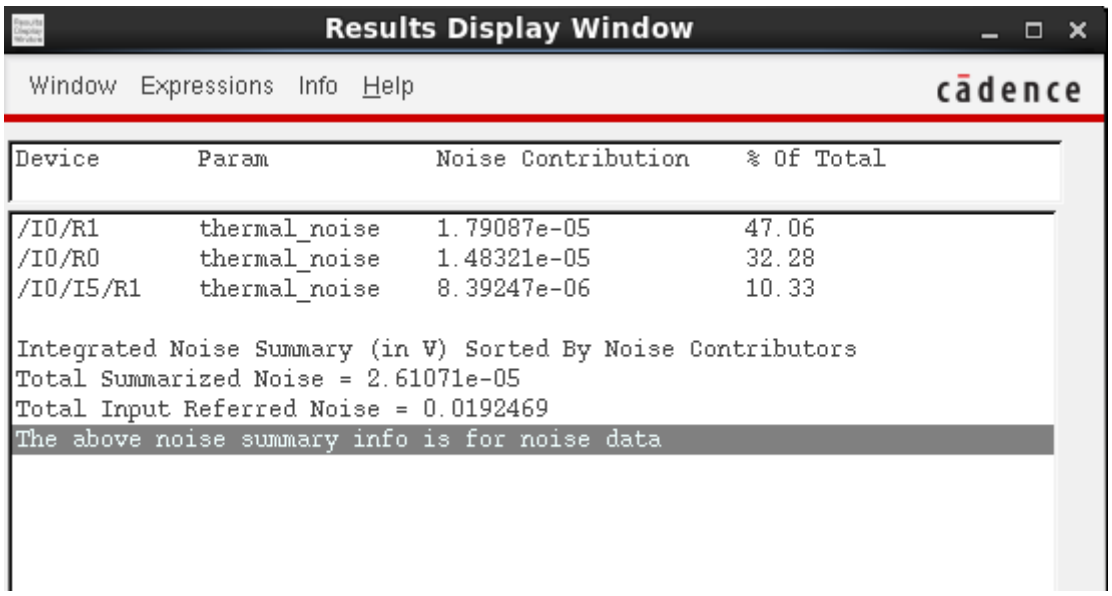

Figure 7. Noise summary of the Nowlin circuit.

2. Jitter Calculation

Jitter can be calculated by the formulae $\sigma_j = \frac{\sigma v}{SR}$.

From figure 7 noise summary $\sigma_v =$ 26.1 µV

By putting the values, $\sigma_j = \frac{26.1\mu V}{103*10^3 V/Sec}$. we get jitter = 253 ps.

CONCLUSION

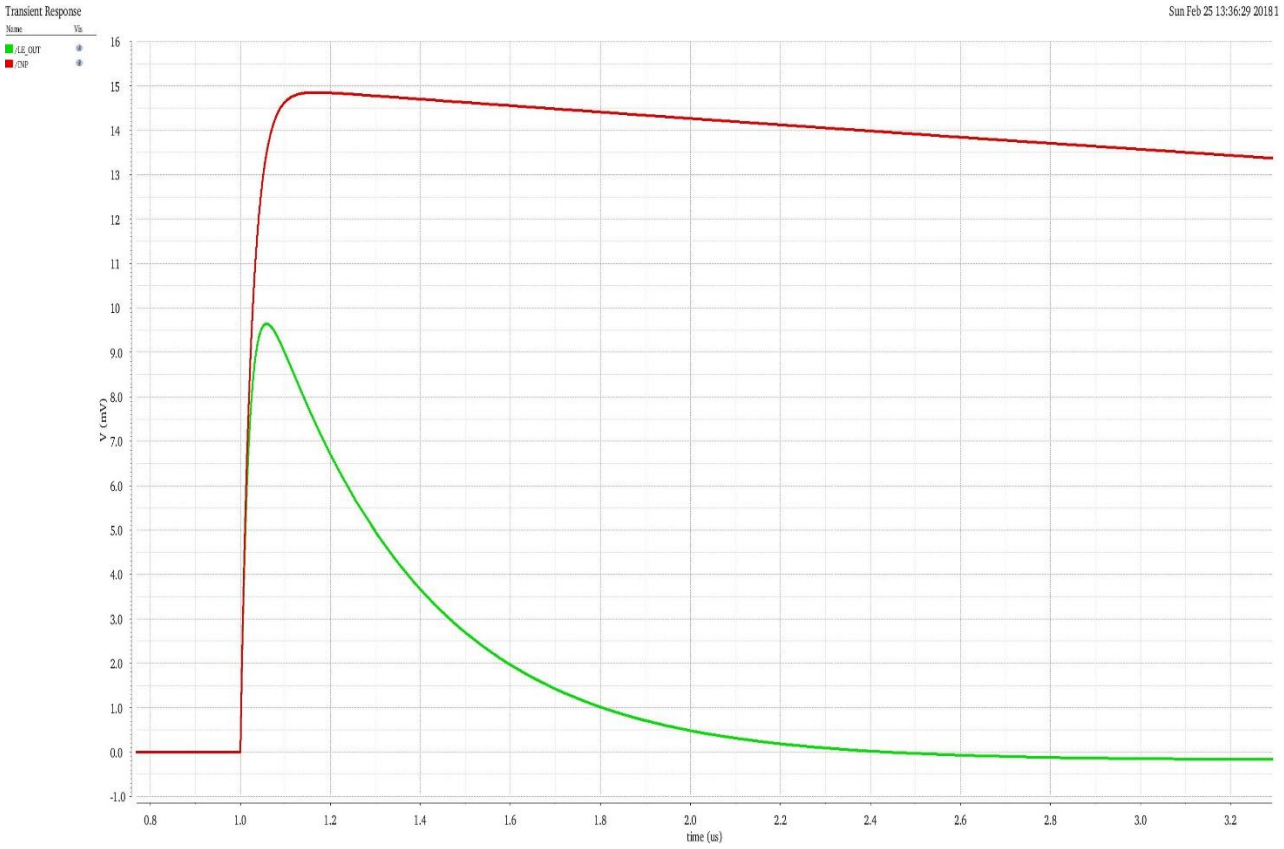

Figure 8. Input signal with 25ns risetime constant along with leading edge output.

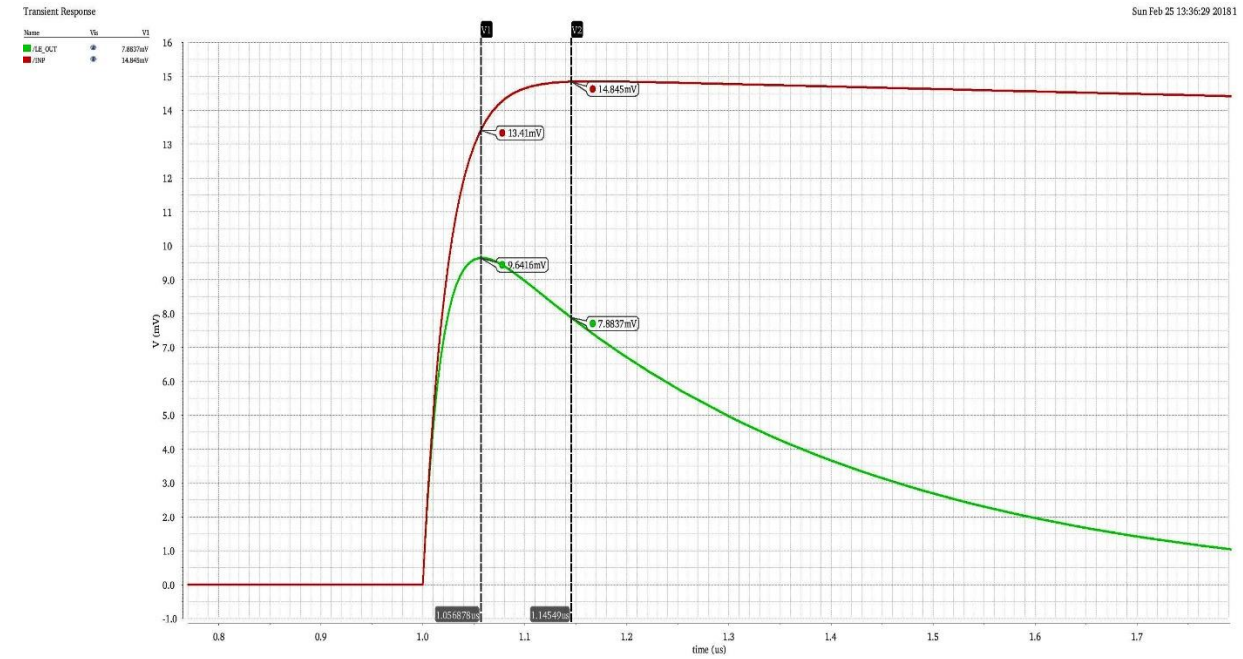

Figure 9. close view of input & output signals showing a difference of factor ~0.7.

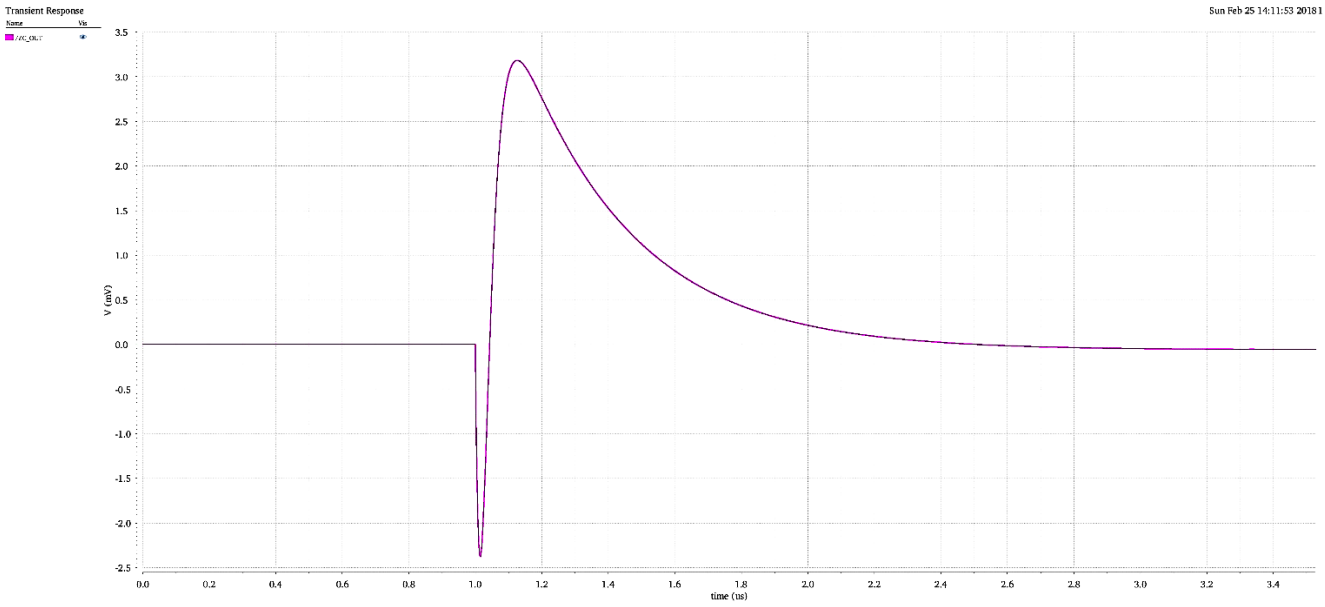

Figure 10. Zero-cross differential output. Time at which signal crosses zero is amplitude independent.

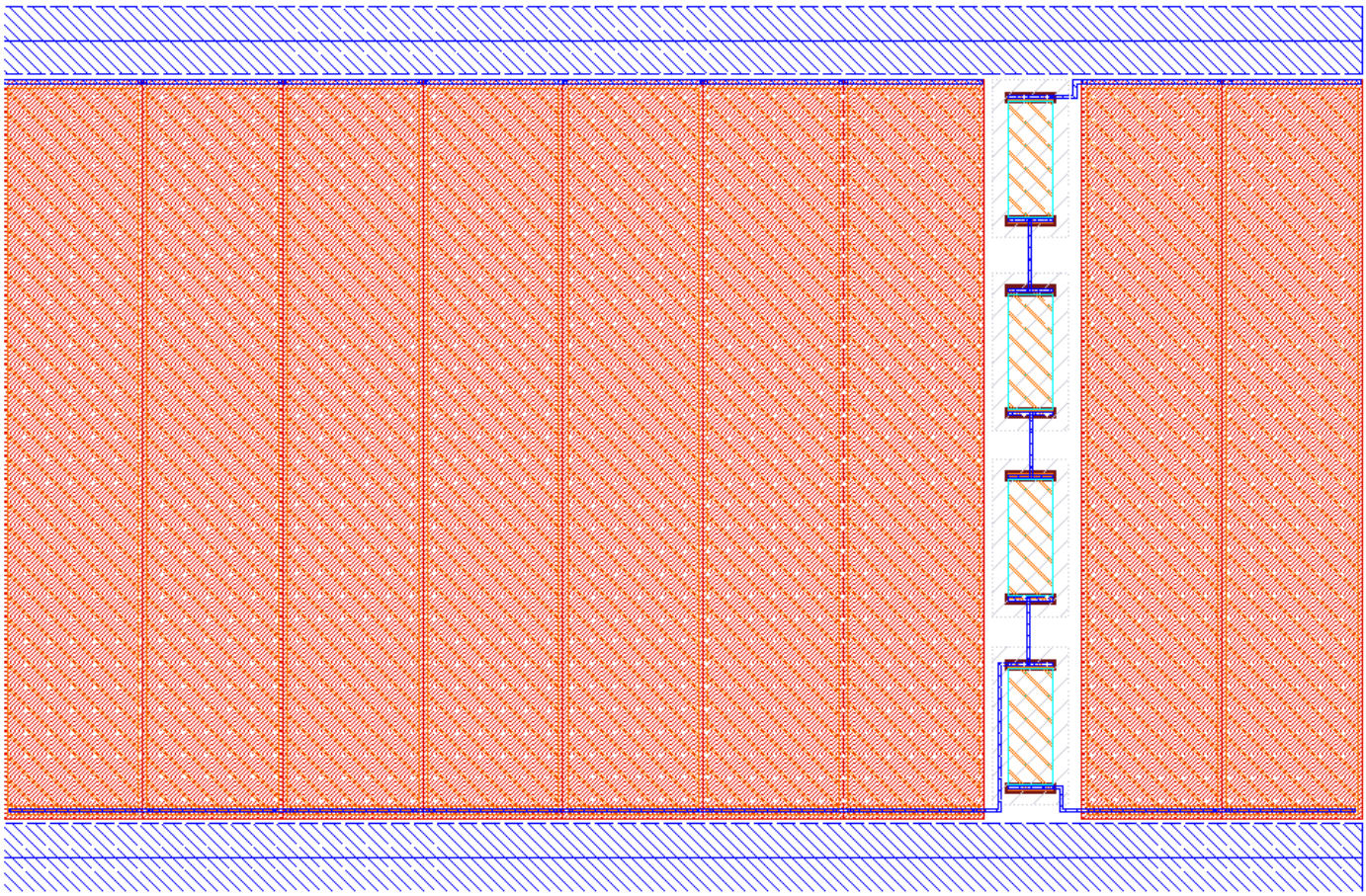

Figure 11. Final layout of Nowlin circuit with dimensions 195µm * 300µm = 58,500µm^2

- ✓ Layout was initially started with a square capacitor, it was observed that square capacitors take more area then the rectangular shape capacitors.
- ✓ Capacitor can be of rectangular shape, if matching is important we can match shape factor of all capacitors to get optimized results.
- ✓ Matching is very important when resistance R_{1A} and R_{1B} is formed. To maintain that we can select the values of all resistance such that all resistances are multiple of some common factor. All the resistances can be implemented using only a single value of resistance.
- ✓ Value of C_1 and C_2 should be selected such that the bigger capacitor can be implemented using parallel connected small value capacitors. We should always try to take unit capacitor between 5-10 pf values to maintain good matching.
- ✓ Finally achieved jitter is 253 ps, which meets the design requirements described in project.