INTRODUCES THE FIRST CAMERA LINK HS AND 10 GIGABIT ETHERNET DEVELOPMENT KIT
**DESCRIPTION:**

The KIT_CLHS is a new camera development kit principally oriented to the Camera Link HS 1.0 protocol. Camera Link HS uses copper and fiber optic connectors and cables that were developed for other standards, such as Ethernet. So the KIT_CLHS can be easily used for 10 Gigabit Ethernet application and offers an effective solution against CameraLink and GigE Vision protocols limitations.

This kit provides all the necessary components to get the development of embedded vision applications started for both M and X protocols. The M protocol uses copper cables for applications up to 2.1GB/s and 15 meters long. Active optical cables (AOC) cables are available for systems requiring longer distances of up to 100 meters. The X protocol (or 10 GigaBit Ethernet) uses fiber optic cables for applications up to 2.4GB/s (2xSFP+ connectors) and 300+ meters long.

It is a powerful tool focus on camera application ensuring that CMOS sensor technologies can be fully exploited while the provided low-power cameras are low-cost and flexible, and data reliability, as requested by the customers, is guaranteed too.

The main advantage of the KIT_CLHS is the cost reduction as the time of development of high-performance camera using the protocol CLHS 1.0 and 10 GbE is shortened. CLHS's IP CORE is available at the AIA and it's evident that IP CORE is enabling the company to save development costs and to shorten development time. Nevertheless, nothing is available as part of the hardware, which is the main advantage of this development kit. Associated with the CLHS IP CORE provided by the AIA, the development kit offers the perfect solution to greatly simplify development.
**TECHNICAL DATA:**

### VIDEO OUTPUT
- **X – PROTOCOL / 10 GBe**
  - 2 x SFP+ connector
  - 3 led's status for each connector
  - 1 led "Loss of signal" per connector.

- **M – PROTOCOL**
  - 2 x CX4 connector
  - 1 for Video transmission with 3 led's status.
  - 1 for loopback test

### INTERFACE
- **5 x HEADER**
  - 1/ 4 x I2S / SMBUS
  - 2/ 7 x Bidirectional TTL
  - 3/ 4 x Photocoupler Input
  - 4/ 4 x Photocoupler Output
  - 5/ 1 x JTAG Header

- **X – PROTOCOL**
  - 10 GBe
- **M – PROTOCOL**
  - 1/ 4 x I2S / SMBUS
  - 2/ 7 x Bidirectional TTL
  - 3/ 4 x Photocoupler Input
  - 4/ 4 x Photocoupler Output
  - 5/ 1 x JTAG Header
- **USB**
  - UART to USB bridge micro AB Connector
- **FMC-HPC (Partially Populated)**
  - 48 differential pairs up to 1.25Gb/s
  - 20 single-ended signals
  - 12C, 12Volts Power
- **POWER**
  - 12V DC ± 10 %
  - ON/OFF 2-pos. slide switch

### MEMORY
- **EEPROM**
  - IIC EEPROM 1Mb
- **FLASH**
  - Quad SPI FLASH 128Mb
- **DDR3L**
  - 4 x DDR3 Low Power 1Gb / 800MHz

### CLOCKING
- Fixed oscillator with differential output
  - 1 x 200MHz (DDR3)
  - 4 x 156.25MHz (GTP’s)
- Fixed Oscillator with CMOS output
  - 1 x 25MHz (GENERAL)

### PHYSICAL CHARACTERISTICS
- **DIMENSIONS**
  - 216 x 133.5 mm
- **WEIGHT**
  - 245 g
- **CERTIFICATION**
  - ROHS compliant with the European Union Directive 2011/65/EU (ROHS2)
  - CE, UL 94 V-0

### CONTROL / DISPLAY
- **PUSH BUTTONS**
  - 8 x User Push Buttons (General use)
  - 1x User Push Button (Program_B)
- **LEDS**
  - 8 x User Leds
  - 8 x Leds (Voltage check)
  - 2 x Leds USB/UART GPIO
  - 2 x Leds FPGA configuration (DONE & INIT_B)

### FPGA
- **XILINX ARTIX-7**
  - Ultra low power FPGA XILINX ARTIX-7 XC7A200T-L2FFG1156E
  - Logic Cell : 215 360
  - DSP Slices : 740
  - Memory : 13 140 kb
HIRES VISION has chosen the ARTIX-7 Xilinx XC7A200T-L2FGG1156 FPGA for its incomparable low-power consumption capacity. This device provides the highest performance-per-watt fabric.

The FPGA speed grade (-2LE) allows the core tension to be set to two different values: 1.0V (high performance) and 0.9v (ultra-low consumption).

With the latter power reduction of 55% in static and 20% in dynamics are possible compared to a standard C grade.

The system allows measuring all the necessary information for its optimization:

Up to 6 power measurements are possible (FPGA consumption measurement, GTP, DDR3L, FMC connector, 3.3V power rail as well as the total power.)

The measurement of temperature (FPGA) and different voltages are also available.

### VCCINT = 0.9v

**ULTRA LOW POWER**

- **GTP**
  - 3.75 Gb/s

- **DDR3L**
  - 667 Mb/s

- **DDR3L TOTAL BANDWIDTH**
  - 2,67 Gb/s - 3,2 Gb/s

**Compared to C-Grade Devices**

- **Static Power Reduction**
  - 55%

- **Dynamic Power Reduction**
  - 20%

### VCCINT = 1.0v

**HIGH PERFORMANCE**

- **GTP**
  - 6,6 Gb/s

- **DDR3L**
  - 800 Mb/s

- **DDR3L TOTAL BANDWIDTH**
  - 2,67 Gb/s - 3,2 Gb/s

- **FMC CONNECTOR**
  - 5,7 Gb/s - 7,5 Gb/s

**Compared to C-Grade Devices**

- **Static Power Reduction**
  - 45%

- **No Dynamic Power Reduction**
Most development kits are centered around a particular component and provide the most generic features possible to reach the highest possible market share. It can therefore sometimes be difficult to find the right card with the desired FPGA/SOC with the necessary resources to fulfill its technical specifications. Sometimes pushing some constraints to use cards featuring expensive components, oversized and not suitable for camera applications.

Our development card is perfectly suited for camera applications. Its FMC connector allows interfacing the card with most of high-resolution or high-speed image sensors. (AMS CMOSIS CMV50000, On Semi VITA 25K, LUXIMA LUX2100...).