MacSpace
-
High Performance DSP for onboard image processing

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The evolution of the Earth Observation mission is driven by the development of new processing paradigms to facilitate:

- Data Downlink
- Data Handling
- Storage

Next generation planetary observation satellites will generate a great amount of data at a very high data rate, for both radar based and optical core applications.
Currently employed applications such as e.g. FFT processing and BAQ compression on SAR satellites that usually do not change during the life-time of a satellite and therefore are mostly realized in hardware (e.g. FPGA accelerators).

More modern applications - due to longer development time and relatively high development costs - can’t be implemented on special purpose hardware accelerators economically!

We have detected the need for a platform that allows:

- Flexibility for space application developers and mission planners
- Still a very high performance comparable to pure hardware implementations
### The role of TU Braunschweig in MacSpace

<table>
<thead>
<tr>
<th>Task</th>
<th>Benchmarking</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lead</td>
<td>TUBS</td>
</tr>
<tr>
<td>Team</td>
<td>DSI, RC, TAS-I</td>
</tr>
</tbody>
</table>

### Jobs to perform

1) Benchmarks to be developed in Software for Simulator and Emulator
2) Integrate Benchmarks with Simulator
3) Integrate Benchmarks with FPGA
4) Measure Performance on FPGA and estimate ASIC performance
5) Apply Algorithmic Optimizations

### Value Proposition
- Creating a framework for performance tests/measurements
- Measuring performance on FPGA
- Compare actual performance to Simulator based estimates
- Perform “Real Application Benchmarks”

### Technical Challenge
- Create software benchmarks
- Integrate and run benchmarks on Simulator
- Integrate Benchmarks for FPGA
- Get the memory footprint
- Measure integer arithmetic performance
- Measure floating point arithmetic performance
- Estimate performance of the real ASIC
System Test Bed

◆ The development of a MacSpace demonstrator is part of the project to validate the usability and functionality of the system.

◆ The processor architecture is implemented in a high-performance FPGA (Xilinx Virtex 7) representing the MacSpace RC64 prototype, which executes the image processing.

◆ A personal computer performs the management and the payload data handling.

◆ The GSEOS V software package is used to send preprocessed radar data, control and monitor the prototype as well as to analyse the results and qualify the performance.
## Target Performance Table of the MacSpace Processor

<table>
<thead>
<tr>
<th>MacSpace Processor: 64 FXD/FP cores, 4 Mbytes*</th>
<th>MacSpace Processor Functions</th>
<th>Performance</th>
<th>Performance / Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>ITAR-Free</td>
<td>Yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Functionality as identified by Joint EC-ESA-EDA task force [EU-2012]</td>
<td>Floating point; Radiation hardness; High-speed interfaces; Interfaces to ADC, DAC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Radiation-Hardness</td>
<td>Rad-hard implementation for total dose hardness, no SEL and high SEU immunity</td>
<td>300 kRad</td>
<td></td>
</tr>
<tr>
<td>High speed interfaces</td>
<td>DDR2/3 interface</td>
<td>25 Gbps</td>
<td></td>
</tr>
<tr>
<td></td>
<td>High-speed serial interfaces</td>
<td>120 Gbps aggregated</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Parallel LVDS interface to ADC/DAC</td>
<td>38 Gbps</td>
<td></td>
</tr>
<tr>
<td>Power</td>
<td>10 w</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock Freq.</td>
<td>300 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GFLOPS (floating point)</td>
<td>38 GFLOPS</td>
<td>3.8 GFLOPS/Watt</td>
<td></td>
</tr>
<tr>
<td>GMACS (16 bit)</td>
<td>75 GMACs</td>
<td>7.5 GMACs/Watt</td>
<td></td>
</tr>
<tr>
<td>GOPS (fixed point)</td>
<td>150 GOPS</td>
<td>15 GOPS/Watt</td>
<td></td>
</tr>
<tr>
<td>ESA benchmark B2 (FFT 4096)</td>
<td>2 Gsps^</td>
<td>200 Msp/Watt</td>
<td></td>
</tr>
<tr>
<td>ESA benchmark B5 (demodulator and filter)</td>
<td>500 Msp^</td>
<td>50 Msp/Watt</td>
<td></td>
</tr>
</tbody>
</table>
Target Performance Table of the MacSpace Processor

- **Available**
- **Future**
- **Cancelled**
- **IP removed**

- **Proton200k**
- **RAD5545**
- **ESA-21469**
- **NGMP-LEON4**
- **SSDP**
- **GR712RC-LEON3**
- **AT6981-CASTOR**
- **Europe**
- **USA**
- **MACSPACE**
- **MAESTRO**

The graph plots the performance of various processors over time, with MIPS/MFLOPS on the y-axis and years on the x-axis.
We do NOT count on 16-bit computations only

- Applications are usually developed on 32-bit and 64-bit processors (mostly Intel x86), before being ported to any kind of space processor
- It’s tough to deal with precision issues of new applications
- Datasets are growing and need larger address space
- Experience shows that industrial players and government agencies do not want to change their algorithms to adapt to special hardware

Quote by US DoE: “We do not put your sh*t into our code!”
We do NOT count on 16-bit computations

Against all odds the RC64 seems to perform unexpectedly well also in 32-bit arithmetics
Microbenchmark Measurements

<table>
<thead>
<tr>
<th>Test No</th>
<th>Name</th>
<th>T1</th>
<th>T2</th>
<th>Total</th>
<th>Iterations</th>
<th>Cycles/s</th>
<th>Cycles/OP</th>
<th>OP/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>B1-1</td>
<td>abs32</td>
<td>599851</td>
<td>681408</td>
<td>81557</td>
<td>10000</td>
<td>300000000</td>
<td>0.81557</td>
<td>367840896.6</td>
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<tr>
<td>B1-2</td>
<td>add32</td>
<td>682244</td>
<td>713799</td>
<td>31555</td>
<td>10000</td>
<td>300000000</td>
<td>0.31555</td>
<td>950720963.4</td>
</tr>
<tr>
<td>B1-3</td>
<td>and32</td>
<td>714654</td>
<td>796674</td>
<td>82020</td>
<td>10000</td>
<td>300000000</td>
<td>0.8202</td>
<td>365764447.7</td>
</tr>
<tr>
<td>B1-4</td>
<td>cnot32</td>
<td>797565</td>
<td>1148055</td>
<td>350490</td>
<td>10000</td>
<td>300000000</td>
<td>3.5049</td>
<td>85594453.48</td>
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<tr>
<td>B1-5</td>
<td>div32</td>
<td>1888720</td>
<td>2009720</td>
<td>121000</td>
<td>1000</td>
<td>300000000</td>
<td>121</td>
<td>2479338,843</td>
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<td>B1-6</td>
<td>mul32</td>
<td>1623576</td>
<td>1786558</td>
<td>162982</td>
<td>10000</td>
<td>300000000</td>
<td>1,62982</td>
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<tr>
<td>B1-7</td>
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<td>1787394</td>
<td>1887732</td>
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<td>1148957</td>
<td>1205631</td>
<td>56674</td>
<td>10000</td>
<td>300000000</td>
<td>0,56674</td>
<td>529343261.5</td>
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<td>B1-9</td>
<td>not32</td>
<td>1206442</td>
<td>1247344</td>
<td>40902</td>
<td>10000</td>
<td>300000000</td>
<td>0,40902</td>
<td>733460466.5</td>
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<tr>
<td>B1-10</td>
<td>or32</td>
<td>1248219</td>
<td>1317271</td>
<td>69052</td>
<td>10000</td>
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<td>0,69052</td>
<td>434455193.2</td>
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<tr>
<td>B1-11</td>
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<td>2011143</td>
<td>2045492</td>
<td>34349</td>
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<td>B1-12</td>
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<td>B1-13</td>
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<td>950720963.4</td>
</tr>
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<td>B1-15</td>
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<td>1553683</td>
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<td>69052</td>
<td>10000</td>
<td>300000000</td>
<td>0,69052</td>
<td>434455193.2</td>
</tr>
</tbody>
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All benchmarks were programmed in C, and compiler optimized.
Modern Synthetic Aperture Radar (SAR) systems are continuously developing:

- higher spatial resolution and new modes of operation
- use of high bandwidths
- combined with wide azimuthal integration intervals

For focusing such data, a high quality SAR processing method is necessary:

- Wavenumber domain (Omega-K) processing is commonly accepted to be an ideal solution of the SAR focusing problem. It is mostly applicable on spaceborne SAR data where a straight sensor trajectory is given.
TU Braunschweig in close connection with the DLR is conducting experimental benchmarks on a representative SAR application excluding preprocessing steps.

The application consists of:

i) Range FFT
ii) Range compression
iii) Azimuth FFT
iv) Modified Stolt Mapping
v) Range IFFT
vi) Azimuth Compression
vii) Azimuth IFFT
SAR Benchmark

SAR Processing is more compute intensive than Hyperspectral Imaging!

It took 47 seconds on an x86 to compute (in double precision) the shown result image (Input data with size of about 500MB).

<table>
<thead>
<tr>
<th>Computation Type</th>
<th>Number of arithmetic computations</th>
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<td>Mixed Radix FFT</td>
<td>~ 50 G</td>
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<td>~ 1.3 G</td>
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Reduction of compute time achievable through:

- Loss in precision (approximated computing)
- Replacing computations through use of Look-Up Tables (LUT)
- Optimized pipelining
- Higher degree of parallelism
Comparison to original results

Shown is the difference of absolute values of complex number results from SAR computation before and after applying approximated computing.

Absolute Value Difference
Comparison to original results

Shown in adjusted scale is the difference of absolute values of complex number results from SAR computation before and after applying approximated computing.

Absolute Value Difference
Comparison to original results

Shown is the phase angle between of complex number results from SAR computation before and after applying approximated computing.

Phase difference
Comparison to original results

Shown in adjusted scale is the phase angle between complex number results from SAR computation before and after applying approximated computing (deviation of 1 degree are acceptable).

Phase difference
Estimated Performance of SAR benchmark

- Computation-wise one single **RC64 chip could be capable of processing SAR data of 8192x8192 complex values** (single precision floating point, i.e. in total 512MB) **in under 2 seconds @ 300MHz**

- 100% compute utilization
- Based on a computation count: 62G Floating Point Operations @ 38 GFLOPS)
- Since the onboard data bandwidth (per core: L1 data – peak 128bit read/write per cycle per core from/to registers, L1 from/to shared memory ('L2') 128bit @~50% utilization read and 32bit write) potentially can sustain the demand by computations, reaching the best-case performance will be a matter of latency hiding.
- In the worst-case scenario, we still expect the application to finish processing the above described data in less than 1 minute.
Thanks for your attention!

ANY QUESTIONS?