Recent Advances in Black Phosphorus-Based Electronic Devices

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The rediscovery of graphene in the recent past has propelled the rapid development of exfoliation and other thin layer processing techniques, leading to a renewed interest in black phosphorus (BP). Since 2014, BP has been extensively studied due to its superior electronic, photonic, and mechanical properties. In addition, the unique intrinsic anisotropic characteristics resulting from its puckered structure can be utilized for designing new functional devices. In retrospect, significant efforts have been directed toward the synthesis, basic understanding, and applications of BP in the fields of nanoelectronics, ultrafast optics, nanophotonics, and optoelectronics. Here, the recent development of BP-based devices, such as nanoribbon field-effect transistors, complementary logic circuits, memory devices, and the progress made in meeting the challenges associated with contact resistance, in-plane anisotropy, and advanced gate stack, are reviewed. Finally, the prospects of 2D materials in meeting the International Technology Roadmap for Semiconductor requirements for the year 2030 are discussed.

1. Introduction

Phosphorus is a fifth group element of the periodic table, which exists in several allotropic modifications. While the first form of elemental phosphorus, referred to as white phosphorus, was already in production as far back as in 1669,[1] black phosphorus (BP) was only discovered by Bridgman in 1914 during an attempt to force ordinary white phosphorus into red phosphorus by high hydrostatic pressure.[2] Subsequent experiments by Bridgman and Jacobs then show this new allotrope of phosphorus to be more thermodynamically stable than white and red phosphorus under 200 and 560 °C, respectively.[3,4] Nevertheless, the interest in black phosphorus fades off gradually. The rediscovery of graphene in 2004 has brought forth a rapid development of exfoliation and other thin layer processing techniques, leading to a renewed interest in black phosphorus. In 2014, experimental works revealing the electronic properties of monolayer and few layers black phosphorus were published.[5,6] Since then, four different material phases of black phosphorus have been predicted by density functional theory.[7] Although black phosphorus, as a layered material, has only become a field of study in recent years, there are already several reviews on the subject covering material properties, fabrication, and devices.[1,8–10] This review provides an updated account of the electronic devices based on black phosphorus.

1.1. Crystal Structure of Black Phosphorus

Although BP is labelled as a 2D material, its structure rather resembles that of an atomic-scale 3D object. A single layer of BP is a double-layered net of phosphorus atoms, as first described by Hultgren et al. in 1935.[11] The crystal structure of black phosphorus has been determined to be orthorhombic with eight atoms per unit cell and lattice parameters, \( a = 3.31 \, \text{Å}, \, b = 4.38 \, \text{Å}, \, c = 10.50 \, \text{Å} \).[12] Like graphite, black phosphorus atoms are strongly bonded in-plane, thereby forming layers, and the layers weakly interact through van der Waals forces. But unlike in graphite, the phosphorus atoms in black phosphorus have five valence shell electrons available for bonding and each phosphorus atom is covalently bonded to three neighboring phosphorus atoms through \( \text{sp}^3 \) hybridized orbitals forming a puckered honeycomb lattice. Each phosphorus atom also has a lone pair, which makes phosphorus very reactive to air. Figure 1 shows the schematic diagram of a black phosphorus crystal structure and compares it to the crystal structure of graphene. This atomic arrangement yields two inequivalent directions within the black phosphorus lattice: the zigzag (parallel to the atomic ridges) and the armchair (perpendicular to the ridges) directions.[10]
1.2. Physical Properties of Black Phosphorus

Bridgman has measured the density (2.69 gm cm\(^{-3}\)) and the compressibility of black phosphorus, and its electrical resistivity as a function of pressure over a limited range of temperature. These measurements have shown that this type of phosphorus is a semiconductor and that it apparently becomes more metallic with increasing hydrostatic pressure, the temperature coefficient of resistivity, between 30 and 75 °C, would reverse sign at 12 000 kg cm\(^{-3}\).[12]

1.3. Electrical Properties of Black Phosphorus

Further measurements of the electrical properties of this material have been conducted by Keyes.[14] The electrical resistivity and Hall conductivity of black phosphorus were measured at a temperature from −195 to 350 °C and its resistivity above 473 K (200 °C) is found to vary as \( \rho = 0.0030 e^{0.33 T} \) Ω cm, where \( T \) is the absolute temperature and \( k \) is the Boltzmann constant in eV K\(^{-1}\). The sign of the Hall voltage indicates that the charge carriers are positive, and its Hall constant \( R_H \) was found to be independent of magnetic field up to 5600 gauss. The concentration of hole carriers calculated from the Hall constant is \( 2 \times 10^{15} \) cm\(^{-3}\) and their mobility varies with temperature as \( \mu = 1.86 \times 10^4 T^{-2} \) cm\(^2\) V\(^{-1}\) s\(^{-1}\). Since the conductivity is essentially intrinsic at high temperature (>150 °C), where the number of hole carriers is equal to the number of electron carriers, we can derive the mobility of the electron carriers by extrapolation. Doing this in the plot of the product of Hall constant and conductivity of the hole carriers against temperature gives us the electron carrier mobility and it is found to vary as \( \mu_e = 1.19 \times 10^7 T^{-2} \) cm\(^2\) V\(^{-1}\) s\(^{-1}\). At room temperature, intrinsic black phosphorus has a resistivity of 1.5 Ω cm, and a carrier mobility of 350 cm\(^2\) V\(^{-1}\) s\(^{-1}\) for holes and 220 cm\(^2\) V\(^{-1}\) s\(^{-1}\) for electrons. The energy bandgap can also be derived from the conductivity measurement at high temperature and is estimated to be \( \approx 0.33 \) eV.[12] This energy gap is found to decrease with decreasing volume of the crystal at a rate of 8.3 eV per fractional change in volume. Finally, it should be noted that the structure of black phosphorus is highly anisotropic and that the electrical properties shown may vary strongly with crystalline direction.[12]

Besides electrical resistivity, Hall conductivity, energy bandgap, hole carrier concentration, and carrier mobilities, Ahmed et al. have also recently calculated the ionization threshold field in hexagonal boron nitride (hBN) encapsulated BP devices.[13] They have found that in contrast to more commonly studied layered semiconducting materials, such as transition metal dichalcogenides (TMDCs), the ionization threshold field in BP (\( \sim 7-5.5 \) V μm\(^{-1}\)) is lower and thus allowing devices based on BP to operate at a bias voltage, where carrier concentration can be increased (e.g., > 9.6 times) via impact ionization, without breaking down. They believe this is also why the saturating behavior in few-layer BP devices is only observed in high-\( k \) and/or thin dielectric environments which induce very strong screening effect but not on substrates with relatively weak charge screening effect such as hBN and SiO\(_2\). They have attributed the lower ionization threshold field found in BP to its lower energy bandgap and higher carrier mobility.

2. Black Phosphorus Electronics Devices

In the past several years, 2D BP has captured the research community’s interest due to its unique electronic, photonic, and mechanical properties. Remarkable efforts have been made regarding the synthesis, fundamental understanding, and applications of BP in the fields of nanoelectronics, nanophotonics, and optoelectronics.[5,6,13–15] In this review, we summarize the recent developments in BP electronics devices, which covers field-effect transistor (FET), complementary logic circuit, memory devices, and printed electronics.

2.1. BP Field-Effect Transistors

The effort in finding new device geometry and alternative channel material has been made in past decades to address the short channel effect in ultrascaled devices. For example, the adoption of tri-gate (FinFET) or ultrathin body transistors has effectively mitigated the issues related to leakage current. However, traditional FETs are still fabricated using 3D semiconductor channels that are made of silicon or III–V semiconductor material, which is limiting its size due to high heat dissipation problems. The emerging 2D materials have therefore provided the opportunities for realizing transistors with ultrathin channels.[16] In FETs with channels made from 2D semiconductors, the leakage current is expected to be effectively suppressed as all electrons/holes are confined in the atomically thin channels. The first work on BP field-effect transistor has reported a direct bandgap of \( \approx 0.2 \) eV and an ultrahigh...
hole field-effect mobility of 1000 cm² V⁻¹ s⁻¹ with a high on/off ratio of ≈10⁵. To date, BP transistor with a minimum channel length of 20 nm has been successfully demonstrated, showing its potential in complying with the 2015 International Technology Roadmap for Semiconductors (ITRS). In this section, we will review the status of BP transistor focusing on the crucial aspect of metal contact, crystalline orientation, gate stack, and nonplanar geometry in the design of a BP FET.

2.1.1. The Effect of Metal Contact in BP FET

Most BP field-effect transistors reported to date show ambipolar electrical transport properties (p-type dominate) because of their small bandgap and Fermi level pinning effect (Figure 2a,b). However, to realize complementary field-effect transistor (a.k.a. complementary metal-oxide-semiconductor (CMOS)), we need the transistor to be unipolar and not ambipolar. Unlike conventional metal-oxide-semiconductor field-effect transistor (MOSFETs), the source and drain of a BP FET are not heavily doped and its semiconductor channel is in direct contact with the metal electrode forming a Schottky contact. As a result, the line-up of the Fermi levels in the metal contacts at the source and drain of the transistor and the semiconductor channel decides to some extent whether the transistor will have an n-type or p-type semiconductor behavior during operation. In other words, one may expect a p-type BP transistor when the metal Fermi level is closer to the valence band and vice versa (n-type) if it is closer to the conduction band.

Various metal contacts have been exploited to improve device performance and modulate BP transistor type. Table 1 shows the various field-effect transistors with different metal contacts that have been reported in the literature. As can be seen in the table, the p-type characteristic is prevalent with high work function metals such as nickel (Ni),[20,21] palladium (Pd),[22] and platinum (Pt)[23] while low work function metals such as titanium (Ti),[5,6] aluminium (Al),[24] or scandium (Sc)[25] resulted in n-type behavior. Besides the work function of the metal contact, the thickness of the BP channel also plays a key role in deciding the final polarity of the transistor as the bandgap of BP is thickness dependent. For example, Perello et al. have shown that a transition from unipolar n-type to ambipolar characteristics occurred when the BP thickness increases from 3 to 13 nm with Al contacts (see Figure 2c). Moreover, BP transistors fabricated by others have also shown different polarity with the same metal contact such as Ti[5,6,26] or Sc[25,27] when the BP channel thickness and the passivation layer are different. Wang et al. have extracted the Schottky barrier height (n-SBH, p-SBH) of Ni, Ag, Ti, Sc, and Er on BP FET with atomic layer deposition (ALD) Al₂O₃ capping layer (see Figure 2d). Their experimental results show that n-SBH and p-SBH are close in value for Ti, Ni, and Ag contacts, which is due to mid-gap Fermi level pinning, while the low work function metals such as Sc and Er have a much lower n-SBH (≈0.1 eV) than p-SBH (≈0.4 eV).

To realize Fermi level depinning and reduce contact resistance, thermal annealing has been proven to be an effective method. Ling et al. have reported that the p-SBH can be reduced from 131 meV to near valence band edge of merely 12 meV after a 300 °C thermal annealing due to the formation of nickel phosphide (Ni₃P) alloy, which serves to improve the Ni/BP interface properties thus leading to Fermi-level depinning.[26] Besides thermal treatment, Liao et al. have also successfully demonstrated a unipolar n-type transport behavior in BP FETs with Ti metal contact by employing 20 nm thick MgO via ALD.[28] Their device exhibits simultaneously a largely improved electron conduction and an almost fully suppressed holes conduction, which they have attributed to a significantly reduced Schottky barrier height for electrons as a result of the MgO.

2.1.2. The Effect of Anisotropy in BP FET

The strong in-plane anisotropy of BP is another important parameter that can influence its mobility.[5,29] The 6–8 times smaller effective mass along armchair direction than zigzag direction is expected to result in a higher hole mobility in the armchair direction.[5] Polarized Raman spectra is a common technique used in the determination of the crystalline orientation in BP. When measured under different sample’s rotation angle, the polarized intensity of the three characteristic Raman phonon modes of BP (A₁g, B₃g, and A₂g) would show different periodic variation under parallel- or cross-polarization configuration.[29–31] As can be seen in Figure 2e, the intensity of the B₃g mode under a parallel-polarization configuration would vary with a period of 90° and the sample’s rotation angle, which gives the minimum intensity, is found to correspond to either armchair- or zigzag-orientation. The exact crystal’s orientation is then confirmed using the intensity of A₂g mode, as it is typically
the strongest along the armchair direction. Xia et al. has also performed an angle-resolved DC conductance measurement and revealed that the hole mobility for a 15 nm BP transistor is 1000 and 600 cm$^2$ V$^{-1}$ s$^{-1}$ in the armchair-direction and zigzag-direction, respectively (Figure 2f).[29] The anisotropic transport properties of BP have also found interesting applications in the field of optical devices[31] and bioinspired electronics.[32]

2.1.3. The Effect of Gate Dielectric in BP FET

In the past decade, the adoption of high-$\kappa$ gate dielectric has been necessary in meeting the scaling requirement of the equivalent oxide thickness (EOT) in CMOS transistor. Although some preliminary BP transistors on thick 90 or 300 nm SiO$_2$ substrate have been realized with high mobility, poor subthreshold
swing (SS) performance of more than 1 V dec\(^{-1}\) is reported. Thus, there is a need for suitable high-\(\kappa\) dielectrics at the gate to improve the device performance in highly scaled transistors. Yang et al. have reported a bilayer gate dielectric of 1.6 nm metal-organic chemical vapour deposition (MOCVD) sp\(^2\)-BN and 1.3 nm ALD Al\(_2\)O\(_3\).[23] A gate leakage of less than 10\(^{-12}\) A \(\mu\)m\(^{-2}\) (\(V_g = -1\) V) and SS as low as 70 mV dec\(^{-1}\) have been achieved with an EOT of 3 nm. Notably, a small hysteresis of 0.1 V is realized, which indicates that BN/Al\(_2\)O\(_3\) is a high quality and scalable gate dielectric as well as an effective passivation layer for BP. The sandwiched thin BN layer effectively blocks the contamination of the H\(_2\)O precursor during the ALD deposition of the gate dielectrics such as Al\(_2\)O\(_3\) or HfO\(_2\), leading to a good interface property.

Hafnium-dioxide (HfO\(_2\)) is another possible high-\(\kappa\) dielectric candidate, which has a dielectric constant of \(\approx 25\). High-performance BP transistors with a thin HfO\(_2\) back gate dielectric have been successfully demonstrated.[31–36] Notably, a hole mobility of \(\approx 536\) cm\(^2\) V\(^{-1}\) s\(^{-1}\) and a near ideal SS of \(\approx 66\) mV dec\(^{-1}\) are achieved simultaneously with an ultrathin 3.4 nm HfO\(_2\) gate dielectric.[34,36] The improved SS performance implies that the ultrathin high-\(\kappa\) gate dielectric provides excellent electrostatic control to the BP channel. Devices at different annealing temperature are also characterized and their SS has shown to have reduced from 76 to 66 mV dec\(^{-1}\) after annealing at 100 °C. The authors attributed the reduced SS to a better BP/HfO\(_2\) interface properties due to the passivation of phosphorus dangling bonds by Hf adatoms as promoted by thermal budget. When subjected to an elevated thermal anneal, however, the large amount of Hf adatoms would cause crystal lattice distortion and impurity scattering effect, leading to degraded device performance. This is evident when the SS of their devices degraded to \(\approx 800\) mV dec\(^{-1}\) at the thermal budget of 200 °C.

### 2.2. BP Complementary Logic Circuits

As one of the basic building blocks for logic circuits realization, complementary inverters using BP as the channel material have stimulated numerous interests for researchers. The complementary inverters constructed by connecting an n-type FET and a p-type FET in series outputs a reversed voltage to the input signal. According to the device structure, the complementary inverters could be classified into two categories, i.e., hybrid complementary inverter and monolithically integrated complementary inverter.

#### 2.2.1. Hybrid BP-Based Complementary Inverter

The hybrid complementary inverter is defined as an inverter consisting of two transistors with two different channel properties. The device structure of the hybrid BP-based complementary inverter consists of a BP nanoribbon FET (BPNR-FET) and a BP nanoribbon transistor with a thin back gate dielectric. The BPNR-FET is used as a bottom gate transistor to provide an additional control over the channel current, while the BP nanoribbon transistor with a thin back gate dielectric is used as a top gate transistor to provide an additional control over the channel current. The hybrid BP-based complementary inverter has been demonstrated to achieve a high hole mobility up to 862 cm\(^2\) V\(^{-1}\) s\(^{-1}\) along the armchair direction (see Figure 2g).[37,38] The BP flake is first mechanically exfoliated onto a SiO\(_2\) substrate before an additional dry etch process using CHF\(_3\)/O\(_2\) gas mixture is performed to sculpture it into nanoribbon array. A 20 nm Al\(_2\)O\(_3\) is subsequently deposited as top gate dielectric to realize both top- and side-wall control to the channel. When compared to a planar BP transistor, the effective width \(W_{\text{eff}}\) of the BPNR-FET is increased to \(W + 2h\) (\(h\) is the thickness of BP films). A sharp decrease in the SS, from 2.69 to 563 mV dec\(^{-1}\), is also observed when the channel width is narrowed from bulk to 60 nm (Figure 2h,i). The mobility of BPNR-FET is found to be width- and thickness-dependent (4–28 nm), with the highest hole mobility of \(\approx 862\) cm\(^2\) V\(^{-1}\) s\(^{-1}\) demonstrated in armchair-oriented device at room temperature by combining high-\(\kappa\) gate dielectric and hydrogen treatment to reduce sidewall scattering. Furthermore, hydrogenation effectively passivates the nanoribbon dangling bonds, leading to hysteresis and contact resistance improvement. Besides, leverage on the black phosphorus nanoribbon structure, the anisotropic thermal transport properties,[39] and tunable anisotropic plasmons has been measured and detected,[40] rendering BP as a more promising anisotropic layered material for future electronics and optoelectronics.

#### 2.2.2. Hybrid Complementary Inverter with Improved Performance

A hybrid BP-based complementary inverter with improved performance has been demonstrated. The device structure of the hybrid BP-based complementary inverter with improved performance consists of a BP nanoribbon FET (BPNR-FET) and a BP nanoribbon transistor with a thin back gate dielectric. The BPNR-FET is used as a bottom gate transistor to provide an additional control over the channel current, while the BP nanoribbon transistor with a thin back gate dielectric is used as a top gate transistor to provide an additional control over the channel current. The hybrid BP-based complementary inverter with improved performance has been demonstrated to achieve a high hole mobility up to 862 cm\(^2\) V\(^{-1}\) s\(^{-1}\) along the armchair direction (see Figure 2g).[37,38] The BP flake is first mechanically exfoliated onto a SiO\(_2\) substrate before an additional dry etch process using CHF\(_3\)/O\(_2\) gas mixture is performed to sculpture it into nanoribbon array. A 20 nm Al\(_2\)O\(_3\) is subsequently deposited as top gate dielectric to realize both top- and side-wall control to the channel. When compared to a planar BP transistor, the effective width \(W_{\text{eff}}\) of the BPNR-FET is increased to \(W + 2h\) (\(h\) is the thickness of BP films). A sharp decrease in the SS, from 2.69 to 563 mV dec\(^{-1}\), is also observed when the channel width is narrowed from bulk to 60 nm (Figure 2h,i). The mobility of BPNR-FET is found to be width- and thickness-dependent (4–28 nm), with the highest hole mobility of \(\approx 862\) cm\(^2\) V\(^{-1}\) s\(^{-1}\) demonstrated in armchair-oriented device at room temperature by combining high-\(\kappa\) gate dielectric and hydrogen treatment to reduce sidewall scattering. Furthermore, hydrogenation effectively passivates the nanoribbon dangling bonds, leading to hysteresis and contact resistance improvement. Besides, leverage on the black phosphorus nanoribbon structure, the anisotropic thermal transport properties,[39] and tunable anisotropic plasmons has been measured and detected,[40] rendering BP as a more promising anisotropic layered material for future electronics and optoelectronics.

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materials. For most of the reported hybrid complementary inverter, transition metal dichalcogenide (TMDs) are selected to be the channel materials, where MoS$_2$\cite{41-45} is selected to be used as the n-FET channel material, while WSe$_2$\cite{45} and MoTe$_2$\cite{44} are selected to be used as the p-FET channel materials, respectively. However, the TMDs-based hybrid inverters suffer from various drawbacks. For example, the devices with a low voltage gain of <1 are not suitable for the demonstration of multistage circuits and most of them are not voltage matched, which would limit their application in cascaded circuits. To overcome these shortcomings, BP is employed to serve as the p-FET channel material to replace the TMDs recently. For example, in 2014, Liu et al.\cite{5} experimentally demonstrated a hybrid inverter using BP and MoS$_2$ as the channel materials as shown in Figure 3. Figure 3a,b shows the structure of the BP/MoS$_2$ inverters. The BP and MoS$_2$ flakes are mechanically exfoliated by scotch tape and then transferred onto the same substrate. The two transistors are connected in series, and the connected drain region is served as the terminal of output voltage $V_{\text{OUT}}$. The inverter shows a clear inversion function with a voltage gain of more than 1 at $V_{\text{DD}} = 1$ V, as shown in Figure 3c.

More recently, Gao et al.\cite{41} proposed an innovative BP/MoS$_2$ hybrid complementary inverter based on a sliding mode triboelectric nanogenerator substrate. The logic circuits could efficiently operate without applying external gate voltage owing to the triloelectric potential produced from the triboelectric nanogenerator, indicating that the BP-based complementary circuits can be further deployed in micro-electromechanical applications.

2.2.2. Monolithically Integrated BP-Based Complementary Inverter

With the progress made in different adatom doping technique, the conductivity of the pristine BP could now be transformed from p-type to n-type via different adatoms such as copper (Cu),\cite{46} potassium (K),\cite{47} aluminium (Al),\cite{48-50} and magnesium oxide (MgO),\cite{28} leading to the realization of complementary inverters based on a single BP channel material.

For example, in a recently reported study, Han et al.\cite{47} has experimentally demonstrated a giant electron doping effect from a thin potassium (K) capping layer that is used to tune the bandgap of BP, thus allowing the conversion of conductivity from p-type to n-type. Figure 4a shows the device structure of the monolithically integrated BP complementary inverter fabricated using this technique. In this figure, the graphene is employed as the bottom gate and the BN is employed as the gate dielectric. Figure 4b shows the optical image of the inverter. The transfer characteristics of the transistors with capped channel, pristine uncapped channel, and uncapped channel with 0.2 nm of K are shown in Figure 4c. The n-type behavior of the transistor is enhanced with the K capping layer, which shows a left-shift in threshold voltage. Figure 4d shows the transfer characteristic of the complementary inverter. A relatively high voltage gain of 5 at $V_{\text{DD}} = 5$ V is achieved. Other than copper and potassium, Chen et al. have also experimentally demonstrated a BP complementary inverter circuit using Al doping technique in transforming the conductivity of BP from p-type to n-type.\cite{49} The circuit structure is shown in Figure 5a. The symmetrical threshold voltage of the transistors is achieved by tuning the concentration of the Al donors, as shown in Figure 5b, ensuring the achievement of voltage matched inverter (Figure 5c). Contact engineering is employed to further enhance the current density of the individual transistors. Low work function metal (i.e., titanium) and high work function metal (i.e., nickel) are selected to be the metal electrodes for n-FET and p-FET, respectively. A relatively low subthreshold swing of $\approx 287.5$ mV dec$^{-1}$ is achieved by employing HfO$_2$ high-k as the gate dielectric, resulting in a relatively high voltage gain of 13 at $V_{\text{DD}} = 2$ V (shown in Figure 5d) for the complementary inverter. The inverter also shows a good immunity to noise. The noise margin for both low and high input voltages is up to 0.27 $V_{\text{DD}}$ (shown in Figure 5e). The relatively large total noise margin indicates that the inverter could be employed to build cascaded circuits. Furthermore, a three-stage ring oscillator with a high oscillation frequency of 1.8 GHz is examined by circuits modelling based on the experimental data (Figure 5f), showing its potential for complex circuit application. Additionally, owing to its unique inherent flexibility, Liu et al. have demonstrated BP complementary inverter on a flexible polyimide (PI) substrate as shown in Figure 5g, in which Al doping technique is employed to transform BP into n-type conductivity.\cite{50} The transfer characteristic of the device shows no significant degradation under the bending radius of 4 and 6 mm (shown in Figure 5h), respectively, indicating the device endurance to mechanical bendability. Besides pure metal, metal oxide such as MgO has also been recently used by Liao et al. in the fabrication of a high-performance unipolar n-type transistor for a fully integrated CMOS BP inverters operating with a low
supply voltage (0.5 V) and without a strict selection of contact metal for n-FET and p-FET of BP.\textsuperscript{[28]} Table 2 summarises the BP-based complementary inverters reported in recent years.

2.3. Exploring BP for Memory Applications

As discussed above, the great potential of BP for electronics application has been extensively explored through the demonstration of FETs and complementary logic circuits. In addition to these devices and modules operating with fixed characteristics, BP, being a promising layered semiconductor, has also been exploited for application in nonvolatile memory and circuits, which are regarded as critical components in many emerging electronic applications including neuromorphic computing, efficient data storage, as well as dynamically reconfigurable digital circuits.\textsuperscript{[51–58]}

Nonvolatile charge-trap memory is a popular type of solid-state memory technology that offers its excellent data storage performance and device scalability. In an early work, by using the ferroelectric copolymer poly(vinylidenefluoride-trifluoroethylene) (P(VDF-TrFE)) as a top gate dielectric, Lee et al. demonstrated a few-layered BP-based memory transistor that exhibited a memory window of 15 V and a program/erase state current ratio of $10^3$ in ambient environment.\textsuperscript{[51]} The two distinctive states (programmed and erased) can be maintained for over 1000 s, clearly manifesting the nonvolatile characteristic of the device. Furthermore, a resistive-load memory inverter and a complementary memory inverter were demonstrated. Floating-gate FET (FG-FET) is a typical configuration of memory device, for which an additional FG is introduced within the gate dielectric of a conventional FET. By storing and releasing charge carriers, the FG enables a shift in the device threshold voltage and subsequent field-effect current modulation (Figure 6a). In the simplest case, a conventional gate dielectric itself with a number of carrier traps can function as both the charge-trapping and charge-blocking layer. Alternatively, a stack of different high-$\kappa$ materials can be employed, and the one with a relatively smaller bandgap can act as charge trapping layer. A typical example is in the work of Feng et al., where nonvolatile BP memory FETs are realized using a gate stack comprising of $\text{Al}_2\text{O}_3/\text{HfO}_2/\text{Al}_2\text{O}_3$.\textsuperscript{[53]} As a result of the difference in electron affinity (2.5 eV for $\text{HfO}_2$ vs 1.0 eV for $\text{Al}_2\text{O}_3$) and in bandgap (4.9 eV for $\text{HfO}_2$ vs 7.7 eV for $\text{Al}_2\text{O}_3$), a potential well for electrons and holes is formed within the gate stack. Consequently, $\text{HfO}_2$ plays the role of charge trapping layer, whereas charge tunneling and charge blocking functions are provided by $\text{Al}_2\text{O}_3$ layers. Additionally, Lee et al. demonstrated a nano floating gate transistor made from BP for nonvolatile memory.\textsuperscript{[54]} Instead of using the dielectric as film-type floating gates, they used gold nanoparticles inside the gate stack for charge trapping purpose, which is expected to deliver superior performance in terms of operation speed, reliability, programmability, and ability to be scaled down. It is worth noting that the aforementioned BP memory transistors have exhibited comparable characteristics, such as a large memory window of greater than 10 V, a long retention time of more than 1000 s, and a respectable on/off ratio above 100 (a summary of reported BP-based memory devices is given in Table 3). In these works, BP is used as channel materials, and the gate stack typically consists of conventional dielectric films such as $\text{SiO}_2$, $\text{Al}_2\text{O}_3$, $\text{HfO}_2$, etc. It is known that the large family of 2D layered materials, whose

![Figure 4. K doping technique. a,b) The structure of BP complementary inverter. c) The comparison after K doping treatment in terms of $I_d$–$V_g$ characteristics. The n-type behavior of the transistor is significantly enhanced with 0.2 nm K layer. d) Transfer characteristic of the BP complementary inverter. A relatively high voltage gain of 5 at $V_{dd}=5$ V is achieved. Reproduced with permission.\textsuperscript{[47]} Copyright 2017, American Chemical Society.](image-url)
electronic properties cover semi-metal, semiconductors, and insulators, have permitted the construction of novel electronic devices. This is also the case for memory cells. For example, the insulating h-BN can be used for charge tunneling layer and semiconducting/metallic 2D crystals are good candidates for charge trapping layers. Among them, layered materials such as...
MoS\textsubscript{2}, graphene, and BP itself have been demonstrated as traps of Si\textsubscript{3}N\textsubscript{4} centers of Si\textsubscript{3}N\textsubscript{4} doping. [52] For example, Li et al. demonstrated nonvolatile current-rectifying characteristic that depends on the graphene semi-floating gate (SFG) and can be modulated by applying voltage pulses to the global control gate. For example, when a negative (positive) voltage is applied to the Si, the BP channel is p-doped (n-doped) due to electrostatic modulation (Figure 6f). Meanwhile, a negative electrical potential exists between the graphene and BP, which will result in holes tunneling from the BP channel to graphene. After the removal of gate voltage (on Si), the tunnel charges are still trapped in the graphene (due to the potential barrier of the hBN), and lead to partially n-doping of the BP channel, forming a p–n junction of BP (BP is intrinsically p-type). Likewise, electrons can also be injected into the SFG by applying a positive control gate voltage, thus forming a p"–p junction of BP. Such nonvolatile programmable property of a semiconducting p–n junction has shown rich potential for diverse applications including photovoltaics, logic rectifiers, and logic optoelectronic circuits. Its nonvolatile properties have also been exploited for novel memory application where the device exhibits \( V_{DD} \) direction-dependent current ratio combined with excellent gate-controllability (Figure 6g).

Using a similar strategy, some other types of BP-based memory devices have also been developed, such as floating-gate manipulated graphene–BP Schottky junction memory and BP p–n–p junction memory. [60, 61] The structures demonstrated in these works, which are distinct from conventional devices, manifest the significant potential held by BP for future functional devices with abundant tunable characteristics and reconfigurable functionalities, including memory devices.

### 2.4. Printed Black Phosphorus Devices and System

To address scalable applications for 2D materials (2DMs), several material production methods have been developed over the last decade. In general, the production methods can be classified either as top-down or bottom-up approaches: 1) top-down process, where bulk layered materials are directly exfoliated to yield monolayer and few-layer flakes, e.g., solution processing. [62] 2) The bottom-up process, where individual flakes are synthesized on substrates, e.g., chemical vapor deposition. [63] In contrast to bottom-up process, top-down solution processing allows exfoliation of monolayer and few-layer 2D material flakes from the bulk in a liquid medium in large quantities for a low setup and production cost. The exfoliated 2D materials are atomically thin and can be easily processed and adapted as active pigments for functional ink formulation, enabling the development of printable applications. [64]

Printed 2DM applications were first reported in 2012, when graphene from liquid phase exfoliation was inkjet-printed to fabricate FETs. [65] Since then, various other 2DMs have also been investigated as active pigments and new functional ink formulations have been reported. [64–70] Table 4 shows all the printable BP applications to date.

---

### Table 2. The benchmark of the BP-based complementary inverters. There are two major types of inverters, including the hybrid inverters and monolithic inverters. All the reported inverters indicate the potential of the realization of high-performance cascaded circuits using BP as the channel material on various substrates.

<table>
<thead>
<tr>
<th>P-FET material</th>
<th>Integration mode</th>
<th>N-FET material</th>
<th>Substrate</th>
<th>Voltage gain</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pristine BP</td>
<td>Hybrid</td>
<td>MoS\textsubscript{2}</td>
<td>Si/SiO\textsubscript{2}</td>
<td>13.8</td>
<td>[41]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HfSiO\textsubscript{2}/Si</td>
<td>V\textsubscript{DD} = 1 V</td>
<td>31</td>
<td>[42]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>HfO\textsubscript{2}/SiO\textsubscript{2}/Si</td>
<td>V\textsubscript{DD} = 1 V</td>
<td>2.8</td>
<td>[43]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SiO\textsubscript{2}/Si</td>
<td>V\textsubscript{DD} = 2.5 V</td>
<td>1.4</td>
<td>[5]</td>
</tr>
<tr>
<td>Monolithic</td>
<td>BP with Cu doping</td>
<td>Graphene/hBN</td>
<td>V\textsubscript{DD} = 2 V</td>
<td>46</td>
<td>[46]</td>
</tr>
<tr>
<td></td>
<td>BP with K doping</td>
<td>Si/SiO\textsubscript{2}</td>
<td>V\textsubscript{DD} = 5 V</td>
<td>5</td>
<td>[47]</td>
</tr>
<tr>
<td></td>
<td>BP with K doping</td>
<td>Si/SiO\textsubscript{2}</td>
<td>V\textsubscript{DD} = 4 V</td>
<td>9.8</td>
<td>[105]</td>
</tr>
<tr>
<td></td>
<td>BP with HfO\textsubscript{2}/Si doping</td>
<td>Al doping</td>
<td>V\textsubscript{DD} = 2 V</td>
<td>13</td>
<td>[49]</td>
</tr>
<tr>
<td></td>
<td>BP with Al doping</td>
<td>graphene/hBN/flexible PI</td>
<td>V\textsubscript{DD} = 3 V</td>
<td>2</td>
<td>[50]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Si/Al\textsubscript{2}O\textsubscript{3}</td>
<td>V\textsubscript{DD} = 1.5 V</td>
<td>5.7</td>
<td>[28]</td>
</tr>
</tbody>
</table>
2.4.1. Formulation of Black Phosphorus Ink for Inkjet Printing

Inkjet printing is a digital, noncontact printing technique where the ink droplets are jetted and deposited in a rapid succession onto the substrate to generate an image. Figure 7a–c schematically presents the two prevalent droplet jetting mechanisms for inkjet: continuous inkjet (CIJ) and drop-on-demand inkjet (DoD). As shown, CIJ is a process where a stream of ink droplets is continuously generated and jetted; In Figure 7a, the droplets charged by the electrode are subjected to an electrostatic field and selectively deflected to deposit onto the substrate. On the other hand, DoD is a process where the ink droplets are only generated when demanded through a piezoelectric or a thermal inkjet process. In a piezoelectric inkjet process...
Table 3. A summary of reported BP-based memory devices.

<table>
<thead>
<tr>
<th>BP device</th>
<th>Charge trapping layer</th>
<th>BP thickness</th>
<th>Substrate</th>
<th>On/off ratio</th>
<th>Retention time</th>
<th>Memory window</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ferroelectric FETs</td>
<td>P(VDF-TrFE)</td>
<td>5–10 nm</td>
<td>285 nm SiO2 on Si</td>
<td>1000</td>
<td>&gt;1000 s</td>
<td>15 V</td>
<td>[51]</td>
</tr>
<tr>
<td>FG FET</td>
<td>MoS2</td>
<td>8 nm</td>
<td>300 nm SiO2 on Si</td>
<td>50</td>
<td>&gt;1000 s</td>
<td>50 V</td>
<td>[52]</td>
</tr>
<tr>
<td>Charge-trap FET</td>
<td>HFO2</td>
<td>15 nm</td>
<td>300 nm SiO2 on Si</td>
<td>100</td>
<td>&gt;1200 s</td>
<td>12 V</td>
<td>[53]</td>
</tr>
<tr>
<td>NFG FET</td>
<td>Au NPs</td>
<td>11 nm</td>
<td>300 nm SiO2 on Si</td>
<td>1000</td>
<td>&gt;10000 s</td>
<td>58.2 V</td>
<td>[54]</td>
</tr>
<tr>
<td>FG FET</td>
<td>BP</td>
<td>7 nm</td>
<td>Glass</td>
<td>1000</td>
<td>&gt;1000 s</td>
<td>22 V</td>
<td>[55]</td>
</tr>
<tr>
<td>Charge-trap FET</td>
<td>Al2O3</td>
<td>5–10 nm</td>
<td>90 nm SiO2 on Si</td>
<td>50 000</td>
<td>&gt;1200 s</td>
<td>16.2 V</td>
<td>[56]</td>
</tr>
<tr>
<td>Synaptic FET</td>
<td>PO2</td>
<td>=20 nm</td>
<td>90 nm SiO2 on Si</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>[52]</td>
</tr>
<tr>
<td>SFG p–n junctions</td>
<td>Gr</td>
<td>5 nm</td>
<td>300 nm SiO2 on Si</td>
<td>10 000</td>
<td>&gt;1200 s</td>
<td>16 V</td>
<td>[59]</td>
</tr>
<tr>
<td>FG Schottky Junction</td>
<td>Gr</td>
<td>9 nm</td>
<td>300 nm SiO2 on Si</td>
<td>10 000</td>
<td>&gt;1200 s</td>
<td>25 V</td>
<td>[60]</td>
</tr>
<tr>
<td>FG PNP junction</td>
<td>Gr</td>
<td>8 nm</td>
<td>300 nm SiO2 on Si</td>
<td>20</td>
<td>&gt;2000 s</td>
<td>38 V</td>
<td>[61]</td>
</tr>
</tbody>
</table>

Table 4. Printable BP applications to date.

<table>
<thead>
<tr>
<th>Printing method</th>
<th>Solvent</th>
<th>Substrate</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inkjet printer</td>
<td>IPA/2-butanol</td>
<td>Si/SiO2, glass, PET</td>
<td>Photodetectors[69]</td>
</tr>
<tr>
<td>Inkjet printer</td>
<td>Acetonitrile</td>
<td>Glass</td>
<td>Humidity sensors[61]</td>
</tr>
</tbody>
</table>
other solvents as summarized in Table 5 by Lin et al., including hexane, iso-propyl alcohol (IPA), methanol, ethanol, acetone, tetrahydrofuran (THF), chloroform, N-methyl-2-pyrrolidone (NMP), 1,2-dichlorobenzene (DCB), N-cyclohexyl-2-pyrrolidone (CHP), N-vinylpyrrolidone (NVP), dimethyl sulfoxide (DMSO), formamide, and water.[73]

Once the pigment of the ink is created, the binder and additive can be added to the sorted BP dispersion to optimize the printing. While most of the solution used in the liquid phase exfoliation of BP can also be used as a solvent for printing, we can tailor the solvent to specific applications via an exchange process described by Hu et al. when BP ink formulated for inkjet printing was first reported in 2017.[69] A key reason for wanting to exchange the solvents used in the report, i.e., NMP and CHP, lies in their high boiling point, which can lead to long drying times when depositing the BP dispersions, resulting in significant oxidation and hence preventing the fabrication of stable devices under ambient conditions. The boiling point of NMP is 204 °C and CHP is 284 °C. Therefore, despite possessing a favorable interfacial surface tension with BP at \( \approx 40 \text{ mN m}^{-1} \) to facilitate exfoliation without reaggregation, the author removed the NMP after exfoliation and redispersed the sedimented BP flakes in IPA and added 2-butanol (10 vol%) to the ink before printing. Moreover, those solvents also do not possess suitable surface tension to wet commonly used substrates such as Si/SiO \(_2\), glass, and polyethylene terephthalate (PET) after deposition, resulting in nonuniform or even discontinuous material deposition. Their binder-free ink suppresses coffee ring formation through induced recirculating Marangoni flow, and supports excellent consistency (<2% variation) and spatial uniformity (<3.4% variation), without substrate pretreatment. Due to rapid ink drying (<10 s at <60 °C), their printing causes minimal oxidation.

Finally, the author did not use any polymer binders in their BP dispersions to resolve the so-called “coffee ring” effect, where flakes, driven by solvent evaporative losses at the droplet edges during drying, concentrate at the droplet edges, compromising printing uniformity. As unlike solvents, binders form an integral part of the printed film, and must be removed through high-temperature annealing or intense pulsed light to retain the functionalities of the 2DMs for electronics devices. This approach is impractical for BP, as it will most likely oxidize it, destroying its electrical properties. Nevertheless, the printed black phosphorus is only stable against long-term (>30 days) oxidation if it is encapsulated with a parylene-C passivation layer.

2.4.2. Fully Inkjet-Printed Black Phosphorus Humidity Sensors

Although there have been numerous demonstrations and device prototypes based on solution-processed 2DMs over the last 10 years, applications based on printed 2DMs inks are only beginning to emerge.[74-84] The key application areas include conductive inks, optoelectronics, sensors, and energy storage, and out of these groups of application, we have a report on a fully printed BP humidity sensors by He et al. in 2018.[85] They have presented a fully inkjet-printed, ultrasensitive humidity sensors with fast dynamic response, using 2D layered structures of either monolayer graphene oxide (GO) or BP as...
sensing materials combined with silver nanoparticle interdigitated electrodes. The BP ink was prepared by sonicating crystalline black phosphorus powder in acetonitrile (boiling point of 82 °C) under a temperature not exceeding 30 °C. After sonication, the dispersion was centrifuged, and the top 10 mL of the dispersion was collected for inkjet printing. As the relative humidity level increased from 11 to 97%, the response capacitance of the BP sensors increased by four orders of magnitude at 10 Hz frequency, which shows ultrahigh capacitive sensitivity factors of 5.08 × 10^4. Moreover, the measured response and recovery time of the BP sensors were found to be 4.6 and 3.0 s (i.e., relative humidity level decreased from 97 to 11%) respectively. Interestingly, their BP film (thickness ≈640 nm and roughness ≈153 nm) is nonuniform and is suffering from “coffee-ring” effect. Both the response time and recovery time of the BP sensors are better than those previously reported for GO, semiconducting TMDC, liquid phase exfoliated BP relative humidity sensors.

As shown in Figure 8, the impedance spectrum obtained from the GO and BP devices is very sensitive to the relative humidity (RH) levels of the environment. The complex impedance spectrum changes from a semicircle to sickle-shaped when the humidity level increased from 11% RH to 97% RH (Figure 8a,b). The impedance spectrum of the BP devices can be modelled by the equivalent circuits shown in Figure 8c (low humidity: 11–43% RH, high humidity: 53–97% RH). Here, R represents the charge transfer resistance, and CPE1 and CPE2 represent constant phase elements, which are used to model the film impedance and electrode/sensing film interface impedance, respectively. They have attributed the decrease in R with increasing RH to the phosphorus oxide (PO_4) formed on the edges of BP flakes. They believe these PO_4 allows the BP nanoflakes to easily bond with water molecules and provide rapid proton conduction pathways. Figure 8e,f shows the typical capacitance response and recovery characteristic curves for the GO and BP humidity sensors. The BP sensor shows a response time of 4.7 s and a recovery time of 3.0 s. In addition, the GO and BP sensors also show excellent repeatability after several cycles (Figure 8g,h).

2.5. Summary and Prospects

The last decade has seen a slowdown in the number of computations that can be performed per kilowatt-hour of electricity consumed, i.e., peak-output efficiency, with each new generation of cutting-edge chips. The inability to increase clock frequencies significantly (maximum frequency achieved by Intel Pentium 4 hovers at 3.5 GHz since 2002), due to the physical limitations of shrinking transistors, has turned chipmakers to make architectural changes—such as putting multiple computing cores in a single microprocessor—but they were not able to maintain historical growth rates. These days, it takes about 2.7 years for peak-output efficiency to double. Historically, a decade of doubling boosted efficiency by a factor of a hundred; at current rates, it would take 18 years to see a hundredfold gain. Fortunately, our computing needs have changed, the emphasis in chip design has shifted from fast central processing units (CPUs) in stationary machines to ultralow-power processing in mobile appliances such as laptops, cell phones, and tablets.

Today, most computers run at peak output for only a small fraction of the time (a couple of exceptions being high-performance supercomputers and Bitcoin miners). Mobile devices such as smartphones and notebook computers generally operate at their computational peak for less than 1% of the time based on common industry measurements. Enterprise data servers spend less than 10% of the year operating at their peak. Even computers used to provide cloud-based internet services operate at full blast for less than half the time. Encouragingly unlike peak-output efficiency, the typical-use efficiency, which is calculated by dividing the number of computations performed over the course of a year by the total electricity consumed, will double every 1.5 years until 2020, putting it back to the same rate seen during the heyday of Moore’s Law.

These gains come from aggressive improvements to circuit design, component integration, and data parallelism, as well as power-management schemes that put unused circuits into low-power states whenever possible. The integration of specialized accelerators, such as graphics processing units and signal processors that can perform certain computations more efficiently, has also helped keep average power consumption down. Of course, as with any exponential trend, this one will eventually end, active power will still be hostage to the physics behind the slowdown in the ability to shrink transistors. Over the next few decades, we will have to rethink the fundamental design of computers if we want to keep computing moving forward at historical rates. In the meantime, steady improvements in everyday energy efficiency will give us a bit more time to find our way.

Compounding the problem of a slowdown in Moore’s Law is the exponential rate of growth in the world’s technological information and communication processing capacities. To put this capacity in perspective, Hilbert and López reported that the 6.4 × 10^18 instructions per second that human kind can carry out on its general-purpose computers in 2007 are in the same ballpark area as the maximum number of nerve impulses executed by one human brain per second (10^17). Although the 2.4 × 10^21 bits stored by humanity in all of its technological devices in 2007 is approaching an order of magnitude of the roughly 10^24 bits stored in the DNA of a human adult, it is still miniscule with respect to the 10^90 bits stored in the observable universe. With the emergence of the Internet-of-Things and cloud technologies, this amount of information is exponentially increasing, creating new challenges for computation and its energy efficiency by generating thousands of trillion of bytes of data by 2030. Therefore, the world’s capacities to sense, transmit, store, and process information will need a technology capable of an improvement of three orders of magnitude or 1000×, in computational performance per Watt.

To address such fundamental problem, new classes of steep-slope switches, e.g., Tunnel FETs, nanoelectromechanical relay, negative capacitance FETs, and metal-insulator-transition, have emerged to drastically lower the supply voltage (V_DD < 0.3 V) and threshold voltage (V_T < 0.1 V) to a level which cannot be reached by CMOS based on 2015 ITRS report. Table 6 below shows the figures-of-merit requested of these new sub-thermionic switches. A recent approach that is different from individually focused technology optimizations is the idea of a monolithically integrated 3D...
Table 6. Targeted figures of merit for new generation of steep-slope switches.\textsuperscript{[90]}

<table>
<thead>
<tr>
<th>Parameters</th>
<th>$SS^a$ [mV dec$^{-1}$]</th>
<th>$I_{on}/I_{off}$ Ratio</th>
<th>$I_{on}$ [mA µm$^{-1}$]</th>
<th>$I_{off}$ [nA µm$^{-1}$]</th>
<th>Operation speed</th>
<th>Performance per Watt</th>
</tr>
</thead>
<tbody>
<tr>
<td>Desired value</td>
<td>10 (over five decades</td>
<td>$10^1$</td>
<td>$0.1$ ($V_{GS} = 0$ V and $V_{DS} = V_{DD}$)</td>
<td>$0.2$ to $1.0$</td>
<td>100s of MHz to 1 GHz</td>
<td>Improved by 10–100 $\times$ vs CMOS for $V_{DD} &lt; 0.3$ V</td>
</tr>
<tr>
<td></td>
<td>of current)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\textsuperscript{a}Subthreshold swing (SS).

---

Figure 8. Nyquist plots of the impedance of a) GO sensor and b) BP sensor at different humidity levels in the frequency range 10 Hz to 1 MHz. ImZ: imaginary part; ReZ: real part. c) Equivalent circuits of the sensor films under low humidity and high humidity. d) Exponential behavior of the Rct parameter versus different humidity levels for the GO and BP sensors. Reproduced with permission,\textsuperscript{[85]} 2018, The Royal Society of Chemistry. The capacitance response and recovery behavior of the e) GO and f) BP humidity sensors at a humidity level between 11% and 97%. Time-resolved response behavior of the g) GO and h) BP humidity sensors at different humidity levels by changing humidity between 11% RH and 97% RH for 5 cycles. All measurements were conducted at 100 Hz and with a bias voltage of 0.5 V. Reproduced with permission.\textsuperscript{[85]} Copyright 2018, The Royal Society of Chemistry.
The authors declare no conflict of interest.

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Conflict of Interest
The authors declare no conflict of interest.

Keywords
black phosphorus, complementary logic circuits, field-effect transistors, gas sensors, memory

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Table 7. Summary of recent progress in BP FET as digital electronics switches.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>SS [mV dec⁻¹]</th>
<th>I_on/I_off ratio</th>
<th>I_off [nA μm⁻¹]</th>
<th>I_on [μA μm⁻¹]</th>
<th>Channel length [nm]</th>
<th>Effective mobility [cm² V⁻¹ s⁻¹]</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Best result</strong></td>
<td>66–69</td>
<td>10³</td>
<td>0.1</td>
<td>0.350</td>
<td>20</td>
<td>800–1000</td>
</tr>
<tr>
<td>2015 ITRS[9] Yr. 2030 HP logic</td>
<td>25</td>
<td>10⁴</td>
<td>100</td>
<td>2.408</td>
<td>10</td>
<td>100</td>
</tr>
<tr>
<td>2015 ITRS[9] Yr. 2030 LP logic</td>
<td>25</td>
<td>10⁴</td>
<td>0.1</td>
<td>1.582</td>
<td>12</td>
<td>100</td>
</tr>
</tbody>
</table>

Scattering-free mobility.

system enabled by Nano-Engineered Computing Systems Technology. It is in this initiative where 2D material like black phosphorus would find its niche application as a high-performance and energy efficient FET. In fact at a common its transport direction outperforms that of monolayer MoS₂ FETs by a factor of 1.57 and 1.89 for n-type and p-type devices and ultrathin body (3 nm) Si FETs (i.e., tri-gate transistor or FinFET) by 1.69 and 2.41, due to highly anisotropic band structure.[97] Although the monolayer black phosphorus is reported to be unstable under ambient conditions, efforts to stabilize BP on greater than 1.5 mA on threshold swing below 60 mV dec⁻¹, a channel length around 10 nm, and a drive current I_on greater than 1.5 mA μm⁻¹. Although theoretical simulation has shown that BP tunneling FET can attain a subthreshold swing below 60 mV dec⁻¹,[100] and the first demonstration of band-to-band tunneling in BP was demonstrated in 2017 by Wu et al.,[100] experimental results reported so far are only comparable to back-gated BP FET on high-x dielectric.[35,101,102]