Depletion effect of polycrystalline-silicon gate electrode by phosphorus deactivation

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1. Introduction

Although metal gate materials with high-k dielectrics were recently introduced in the CMOS (complementary metal-oxide-semiconductor) industry, polycrystalline silicon is still widely used as gate electrode due to the efficiency and simplicity of its manufacturing process and application [1–3]. However, one of the major limitations in the extensive use of polysilicon as an electrode is the polysilicon depletion effect (PDE), which is generated by an applied bias on the polysilicon electrode. The resultant depletion layer causes an increased gate dielectric thickness and influences other device characteristics such as reduction of device current. The depletion layer width (W_d) resulting from the PDE can be expressed by the following equation [4]:

W_d = \sqrt{\frac{2K_S\varepsilon_0}{qN}} \phi_s

where K_S is the semiconductor dielectric constant, \varepsilon_0 is the permittivity of free space, N is the effective doping concentration, and \phi_s is the potential difference between the bulk and the surface of the semiconductor. According to Eq. (1), one of the major factors that determines the depletion width is the effective doping concentration of polysilicon. Usually highly doped polysilicon is used for a metal electrode; hence, an increase of depletion width could be generally negligible. However, a change of design rules in CMOS technology leads to a reduction in gate channel length and gate electrode size. As a result, the PDE is no longer an insignificant problem [5–9]. For example, in a flash memory device in which the floating gate contains polysilicon, the PDE increases as the floating gate volume decreases [10–12]. When conducting program and erase operations, the polysilicon depletion layer is generated on the surface between floating gate and tunnel oxide by a strong electric field [13,14]. This polysilicon depletion layer causes the deterioration of device features such as coupling ratio or uniformity.

In this paper, the effect of the thermal process on the PDE was systematically investigated in order to study the mechanism of the PDE. It was found that the major reason for the polysilicon depletion effect is not the out-diffusion of phosphorus but the electrical deactivation of phosphorus, which might be segregated into grain boundary. Therefore, by increasing the size of polycrystalline silicon grain, we can efficiently reduce the polysilicon depletion effect and enhance the tolerance to deactivation.

2. Experimental

For an investigation of the PDE after annealing, metal-oxide-silicon (MOS) structures were prepared as follows: 50 Å thick


SiO₂ was deposited onto a p-type Si wafer by low pressure chemical vapor deposition (LP-CVD) at deposition temperature of 830 °C using dichlorosilane [SiCl₂H₂] as a precursor. Then, amorphous silicon (a-Si) was formed on top of it using LP-CVD at deposition temperature of 530 °C with an in-situ phosphorus doping concentration adjusted through the flow control of PH₃. Sequential thermal processes in a furnace at 900 °C for 60 min in an N₂ ambient and in a rapid thermal anneal (RTA) furnace at 900 °C for 90 s in an N₂ ambient were conducted for crystallization of deposited phosphorus-doped polysilicon and dopant-activated silicon, respectively. Through these processes a Si-sub/SiO₂ 50 Å/Poly-Si 2000 Å stack was formed. To investigate the change in phosphorus concentration by a subsequent thermal process, a two-step post RTA was applied, denoted by RTA-1 and RTA-2, which is described in Fig. 1(a). In addition, in order to change the grain size of polysilicon, a pre-crystallization thermal process by RTA was applied to another group of samples before the crystallization thermal process as described in Fig. 1(b). For preparing a capacitance-voltage (CV) measurement sample, 100 Å thick SiO₂ and 2000 Å thick poly-Si layers were added on the above-mentioned stack as a dielectric and top electrode, respectively. Then, through the etching of upper polysilicon, a 100 nm x 100 nm sized test pattern was defined and a CV measurement to determine the polysilicon depletion width was conducted using an Agilent E4980A precision LCR meter. A CV measurement was conducted at high frequency of 100 kHz and signal amplitude of 50 mV. To determine the electrically activated phosphorus concentration, sheet resistance (Rₛ) measurements and the physically incorporated P-conc. by SIMS. The change of relative P-conc. values is illustrated in Fig. 2. Before the thermal process, the physically incorporated P-conc. of all samples were fixed at approximately 1.23 x 10²⁰ cm⁻³. As shown in Fig. 2, relative P-conc. values determined by Rₛ after post RTA-1’s of 600, 700, and 800 °C decreased to 95–97%, which were relatively lower than that of approximately 99% and nearly 100% after annealing at 500 °C and 900 °C, respectively. This means that annealing temperature is not the main cause of electrically activated P-conc. change in highly doped polysilicon. Meanwhile, physically incorporated P-conc. values measured by SIMS were almost the same in all samples, even though electrically activated P-conc. values determined by Rₛ showed different values. This means only electrically activated P-conc. is changed by post RTA-1 without a change of the physical amount of phosphorus in polysilicon. On the other hand, the P-conc. values obtained were almost 100% post RTA-2 (900 °C, 90 s). These results indicate that the major cause of electrically activated P-conc. change by thermal treatment is not the out-diffusion of dopants but electrical deactivation. To understand the PDE phenomena fundamentally, the cause of electrical deactivation of phosphorus should be determined. Accordingly, we focused on the mechanism study of electrical phosphorus deactivation, which is the major reason for the PDE at high doping density.

As discussed above, phosphorus loss after RTA-1 determined by SIMS was negligible and re-activation of the dopant occurred in the post RTA-2. Therefore, it is expected that deactivated phosphorus exists on the interstitial site inside the polysilicon grain or in the grain boundary as a segregated form [15–18]. To confirm how the deactivated phosphorus exists, we compared the deactivation degree among polysilicon samples of different grain size because the different proportion of grains and grain boundaries might lead to different degrees of phosphorus deactivation. The polysilicon samples with different grain sizes were prepared by the formation of a crystallization seed through the additional thermal process (described as “Pre-crystallization thermal” in Fig. 1(b)) at a different temperature before applying the crystallization thermal process [19]. Through TEM and TEM-SAD patterns, as shown in Fig. 3, it was confirmed that the grain size became smaller as the pre-crystallization temperature increased. It seems the pre-crystallization thermal process results in more crystallization nuclei and leads to an increase of the density of grains and grain

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**Fig. 1.** Schematic thermal process sequence of samples (a) to investigate the phosphorus concentration change and (b) to differentiate the grain size.
limit. Compared to this previous report, although notable segregated into the poly-Si grain boundary under the solubility et al., and it was observed that the phosphorous atoms could easily poly-Si was investigated using atom probe tomography by Han process. In the previous report, the phosphorous diffusion path in an activated state again by applying the high temperature thermal phorus by the subsequent thermal process can be converted to/C176gated phosphorus is re-dissolved at its solid-solubility level at conc. values of all samples were recovered. This is because segre-while, when applying post RTA-2, the electrically activated P-conc. change because the solid-solubility level was high enough. Mean-

boundaries. To investigate the relationship between the density of grain boundaries and the electrical deactivation of phosphorus, pre-crystallized polysilicon samples (pre-crystallization temperature of 500–800 °C) were annealed at 600 °C, 90 s (RTA-1) for the deactivation of phosphorus. Fig. 4 shows the plot of the change in XRD FWHM and electrically activated P-conc. determined by Rs. It was observed that there was a reasonable correlation between the grain size and deactivation: as the grain size decreases, so does the relative electrically activated P-conc. These observations indicate that the deactivation of phosphorous in polysilicon occurs more when the density of grain boundaries increases and phosphorus deactivation inside poly-Si occurs by grain boundary segregation [16,17]. Through the above mechanism, the change of electrically activated P-conc. in highly doped polysilicon samples can be explained as follows: The phosphorus in polysilicon grain is segregated into grain boundaries by the gap of solubility in the case of post RTA-1 in the temperature range of 600–800 °C; hence, the electrically activated P-conc. is reduced [15]. Additionally, the reason for the high electrically activated P-conc. value of post RTA-1 at 500 °C might be that the temperature might not be high enough for segregation to occur and the phos-phorus remains in grain form rather than segregate at the grain boundary. In case of post RTA-1 at 900 °C, there was no notable change because the solid-solubility level was high enough. Meanwhile, when applying post RTA-2, the electrically activated P-conc. values of all samples were recovered. This is because segre-gated phosphorus is re-dissolved at its solid-solubility level at 900 °C and is reactivated. This means that the deactivated phosphorus by the subsequent thermal process can be converted to an activated state again by applying the high temperature thermal process. In the previous report, the phosphorus diffusion path in poly-Si was investigated using atom probe tomography by Han et al., and it was observed that the phosphorous atoms could easily segregated into the poly-Si grain boundary under the solubility limit [20]. Compared to this previous report, although notable change of P-conc. by segregation is not observed under at post RTA-1 at 900 °C in our study, it is obvious that phosphorous segregation into grain boundary is affected by the change of solid solu-bility and grain size. Consequently, the PDE caused by phosphorus deactivation can be reduced by minimizing the grain boundary through increasing the grain size of polysilicon and by reactivating the segregated phosphorus by applying a high temperature thermal process.

Finally, the comparison of polysilicon depletion width for two samples, which have different grain sizes, was conducted to confirm the PDE reduction. To prepare polysilicon samples, which differentiated the grain size, pre-crystallization thermal processes were applied at 900 °C and 500 °C. Depletion width of polysilicon was determined for the metal-insulator-metal capacitor structure as mentioned in the experimental section. When a certain level of inversion bias is applied on the upper electrode, a depletion region is induced on the poly-Si/SiO2 surface and this increases equivalent oxide thickness, which is indicated by a capacitance drop. Therefore, the relative depletion width can be calculated from capacitance drop such that $C_{\text{inv}}/C_{\text{max}}$, where $C_{\text{max}} \approx C_{\text{ox}}$ [5], where $C_{\text{inv}}$, $C_{\text{max}}$, and $C_{\text{ox}}$ are the inversion capacitance, maximum capacitance and oxide capacitance, respectively. As shown in Fig. 5, small grain sized samples had much larger depletion width than large grain sized samples despite having the same physically incorporated phosphorus concentration of $1.23 \times 10^{20}$ cm$^{-3}$ measured by SIMS. It is obvious that electrical activation of phosphorus is obstructed when the density of grain boundaries is increased.

4. Conclusions

The main cause of the PDE by the subsequent thermal process is phosphorous deactivation in highly doped polysilicon. The mechanism of the PDE in highly phosphorus-doped polysilicon is phosphorous deactivation caused by the segregation of phosphorus,
which is segregated at the grain boundary. Therefore, PDE can be effectively suppressed by enlarging the grain size of poly-Si.

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