

# Smart Mobility ARChitecture

## Hardware Specification Errata Document



# 1 Introduction

## 1.1 LEGAL

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## 1.2 REVISION HISTORY

Rev	Date	Originator	Notes
0.1	Dec. 16, 2016	M. Unverdorben	Initial release
1.0	Jan. 12, 2016	M. Unverdorben	Finalized without changes in the content
1.1	Feb. 09.2016	M. Unverdorben	Added Errata 2-4

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## 2 Erratum 1: Interchanged Pins on SPI1

Applies to SMARC Hardware Specification V2.0

### 2.1 MOTIVATION

When outlining the update for the SPI1 to eSPI two pins have been interchanged (MISO and MOSI). The pin-out table in chapter 5.1 and the pin-out comparison in chapter 10.1.1 need to be corrected.

### 2.2 CORRECTIONS IN THE SPECIFICATION

#### 2.2.1 CHAPTER 5.1 – PAGE 45

##### Wrong in Specification 2.0

P57	ESPI_IO_0
P58	ESPI_IO_1

##### Correction for Specification 2.0

P57	ESPI_IO_1
P58	ESPI_IO_0

#### 2.2.2 CHAPTER 10.1.1 – PAGE 74

##### Wrong in Specification 2.0

P57	<del>SPI1_DIN</del>	ESPI IO 0
P58	<del>SPI1_DO</del>	ESPI IO 1

##### Correction for Specification 2.0

P57	<del>SPI1_DIN</del>	ESPI IO 1
P58	<del>SPI1_DO</del>	ESPI IO 0

### 3 Erratum 2: Wrong Description about Coupling Capacitors for USB 3.0 SSTX Signals

Applies to SMARC Hardware Specification V2.0

#### 3.1 MOTIVATION

Chapter 4.10.2 describes the USB 3.0 signals. Due to a copy and paste error the Description of SSTX signals is misleading

#### 3.2 CORRECTIONS IN THE SPECIFICATION (CHAPTER 4.10.2 PAGE 30)

##### Wrong in Specification 2.0

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USB[2:3]SSTX- USB[2:3]SSTX+	Output	USB SS	Transmit signal differential pairs for SuperSpeed USB data Coupling caps for <b>RX</b> pairs are <b>off</b> -Module
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##### Correction in Specification 2.0

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USB[2:3]SSTX- USB[2:3]SSTX+	Output	USB SS	Transmit signal differential pairs for SuperSpeed USB data Coupling caps for <b>TX</b> pairs are <b>on</b> -Module
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## 4 Erratum 3: Misleading Table Structure for PCIe

Applies to SMARC Hardware Specification V2.0

### 4.1 MOTIVATION

Chapter 4.11.1 describes the link width for PCI Express lanes. One line in the table is misleading and should be corrected:

### 4.2 CORRECTIONS IN THE SPECIFICATION (CHAPTER 4.11.1 PAGE 32)

#### Wrong in Specification 2.0

SMARC PCIe Lane	Possible Link Configuration			
PCIe A	x1	x1	x2	x4
PCIe B	x1	x1		
PCIe C	x1	x2	x2	
PCIe D	x1			

#### Correction in Specification 2.0

SMARC PCIe Lane	Possible Link Configuration			
PCIe A	x1	x1	x2	x4
PCIe B	x1	x1		
PCIe C	x1	x2	x2	
PCIe D	x1			

## 5 Erratum 4: Wrong Signal Description for Alternative MIPI-CSI3 Usage

Applies to SMARC Hardware Specification V2.0

### 5.1 MOTIVATION

Chapter 5.1 points out the module pin out. For an alternative usage of MIPI-CSI3 signals the naming of two pins has been interchanged.

### 5.2 CORRECTIONS IN THE SPECIFICATION

#### 5.2.1 CHAPTER 5.1 - PAGE 44

##### Wrong in Specification 2.0

S5	CSI0_TX <del>-</del> / I2C_CAM0_CK
S7	CSI0_TX <del>-</del> + / I2C_CAM0_DAT

##### Correction in Specification 2.0

S5	CSI0_TX <del>-</del> + / I2C_CAM0_CK
S7	CSI0_TX <del>-</del> / I2C_CAM0_DAT

#### 5.2.2 CHAPTER 10.1.1 – PAGE 76

##### Wrong in Specification 2.0

S5	I2C_CAM_CK	CSI0_TX <del>-</del> / I2C_CAM0_CK
S7	I2C_CAM_DAT	CSI0_TX <del>-</del> + / I2C_CAM0_DAT

##### Correction in Specification 2.0

S5	I2C_CAM_CK	CSI0_TX <del>-</del> + / I2C_CAM0_CK
S7	I2C_CAM_DAT	CSI0_TX <del>-</del> / I2C_CAM0_DAT