Executive Summary - XYZ Corporation

The Unmet Need

Complex integrated circuits called System on a Chip (SoC) devices are at the heart of today's high-technology products such as cell phones, personal digital assistants, digital cameras, ink jet printers, consumer audio and video products, and computers. Competitive pressure and customer requirements result in SoCs often being priced under $10 – or, increasingly, even under $2.

Test is becoming the dominant cost factor in SoC manufacturing, but test is beginning to undergo a revolution that promises to reduce test cost to a fraction of its current level, making lower-cost SoC devices practical. That revolution is based on the Design for Test (DFT) technologies being used today to shorten SoC time-to-market by several months DFT technologies have a hugely important side effect: they allow complex SoC devices to be tested with a simple tester that is 1/10th the cost of traditional testers.

The Solution

Our opportunity is to lead the transition of the SoC test market from multi-million dollar ATE that live almost exclusively on the test floor, to $100,000 production test solutions and fully compatible $50,000 engineering test solutions. Although these prices are much lower than the price of today's testers, our volume potential is greatly increased because we are targeting engineering test as well as the more traditional production-test application. In addition, lowering the cost of test – the dominant SoC cost – will enable the SoC industry to enter new, low-cost SoC markets, increasing SoC unit volumes. That drives the need for more low-cost testers.

XYZ's first product, the ABC 500™, is targeted to validation of DFT tests and will be used by engineers in a lab environment. The ABC 500 will enter Beta test in early Q4 of 20xx, with production release in December.

Proof of Concept

The feasibility of testing complex SoC devices with a simple tester isn't just a theory – IBM and Texas Instruments do it today with low-cost testers they designed themselves. Neither company is particularly interested in being a tester vendor – and they, together with the other major integrated circuit vendors, are looking for someone to provide a low-cost solution commercially. IBM, Texas Instruments, Motorola, Infineon, Philips, ST Microelectronics, LSI Logic, Toshiba, and other major integrated circuit vendors believe that a low-cost DFT Tester is a strategic imperative for the SoC business. market size.

The new generation of 300mm fabs and growth in the current generation of 200mm fabs will drive a demand for $1-2 billion in DFT-focused SoC testers by 2005. Just a single 300mm SoC fab will require hundreds of testers.

Competition

Existing tester vendors will not meet the DFT Test need because their business models are structured around multi-million dollar testers. Just as PCs displaced the minicomputer market, DFT-focused testers will displace a significant fraction of the $5 billion SoC tester market – an ideal opportunity for a startup.

XYZ Corporation

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Team

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<name> CTO, Lorem ipsum dolor sit amet, consectetur adipiscing elit, sed do eiusmod tempor incididunt ut labore et dolore magna aliqua. Ut enim ad minim veniam, quis nostrud

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Exit Strategy

We believe that the growth potential presented by the DFT Test opportunity will allow us to prepare XYZ for an Initial Public Offering of stock. We also believe there are shorter-term exit strategies that involve proving our solution and then selling XYZ to either a tester company or a device handler/ prober company.

Financial Summary

As of mid 20xx, XYZ's monthly burn rate is $230,000 with 16 employees, various contractors, and outsourced services (board building, etc.) Burn rate will ramp to $275,000 in Q4. Expectations for 20xx income are shown in the following table.

20xx Income Projection
Engineering Test
($ in 000)

	Q1	Q2	Q3	Q4	Tot
Revenue	800	1200	2100	3400	7500
G. Margin	560	840	1470	2380	5250
Expense	1000	1070	1310	1630	5010
EBIT	**(440)**	**(230)**	**160**	**750**	**240**

2003 revenues are based on sales of the ABC 500. Net monthly burn for engineering test in 20xx will improve from $367,000 outflow in Q1 to $67,000 outflow in Q4.

In 20xx, we will begin investing in a second development team to create a product targeted to wafer-level production testing. Expenses for the wafer test product are not shown in the above income statement. The wafer test development will be funded by a Series C round in 20xx.

Funding

XYZ closed $4.25 million of Series A investment in September of 20xx to fund development of the ABC 500. Investors included Smartforest Ventures, Ridgewood Capital, Synopsys, Empire Ventures, PacRim Venture Partners, and Agilent Corporation.

We are seeking a Series B investment of $3 to $4 million in funding to roll-out the engineering test product, and to provide adequate runway to put us in a strong position for the Series C round in 20xx.

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